ispMACH™ 4A Family Architectural Description

ispMACH4A Family Introduction

The fundamental architecture of ispMACH 4A devices (Figure 1) consists of multiple optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

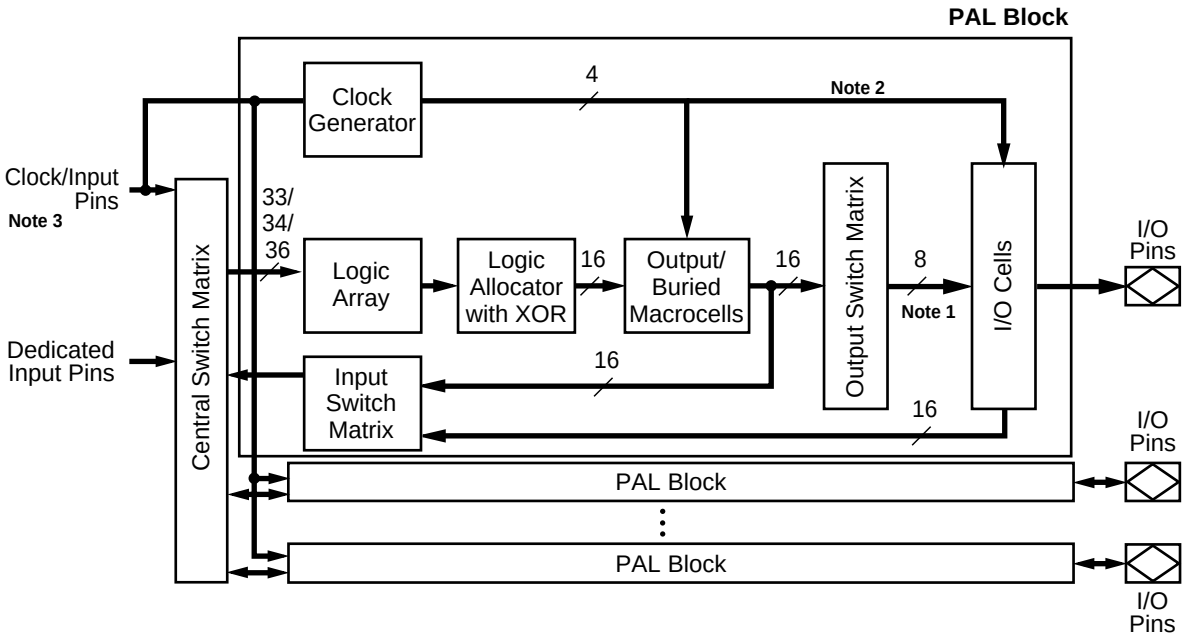
The key to effective use of these devices lies in the interconnect schemes. In the ispMACH 4A architecture, the macrocells are flexibly coupled to the product terms through the logic allocator and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

The macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 1).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in ispMACH 4A devices communicate with each other with consistent, predictable delays.

The central switch matrix makes an ispMACH 4A device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Figure 1. ispMACH 4A Block Diagram and PAL Block Structure



Notes:

1. 16 for ispMACH 4A devices with 1:1 macrocell-I/O cell ratio (see next page).
2. Block clocks do not go to I/O cells in M4A(3,5)-32/32.
3. M4A(3,5)-192, M4A(3,5)-256, M4A3-384, and M4A3-512 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.

Table 1. Architectural Summary of ispMACH 4A Devices

	ispMACH 4A Devices	
	M4A3-64/32, M4A5-64/32 M4A3-96/48, M4A5-96/48 M4A3-128/64, M4A5-128/64 M4A3-192/96, M4A5-192/96 M4A3-256/128, M4A5-256/128 M4A3-384, M4A3-512	M4A3-32/32 M4A5-32/32 M4A3-256/160 M4A3-256/192
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

Each PAL block consists of:

- Product-term array
- Logic allocator
- Macrocells
- Output switch matrix
- I/O cells
- Input switch matrix
- Clock generator

ispMACH 4A Timing Model

The primary focus of the ispMACH 4A timing model is to accurately represent the timing in an ispMACH 4A device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i." By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized ispMACH 4A timing model is shown in Figure 2. Refer to the application note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

ispMACH 4A and MACH 4 Device Differences

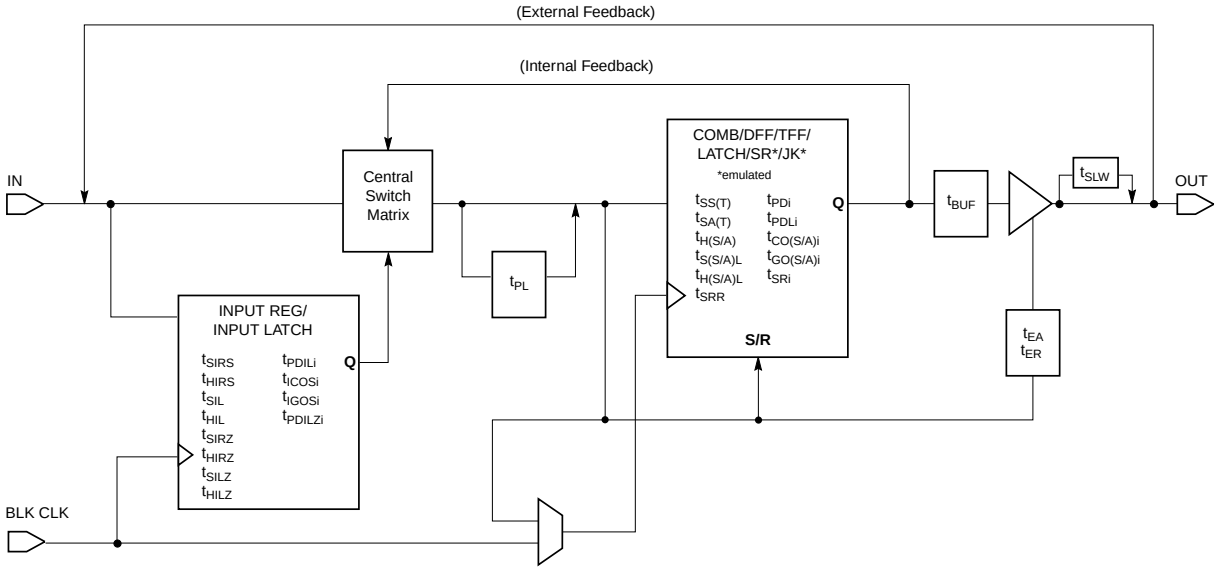
The ispMACH4A and MACH® 4 product families are identical in basic function and have identical end-use environmental specifications. The ispMACH 4A family possesses significant advantages over the MACH 4 family in both performance and ease of use. Design differences give the ispMACH 4A products programmable pull-up or Bus-Friendly™ inputs and I/Os not found in the MACH 4 family. The ispMACH 4A family design also allows hot socketing with leakage and loadings on I/O pins comparable to normal background leakages of tri-stated pins. The ispMACH 4A devices are manufactured on the 0.25µm Leff EE8 wafer fab process that makes a faster transistor due to the shallow junctions and smaller Leff. The MACH 4 devices are manufactured on the 0.35µm Leff EE7 process. The ispMACH 4A family, with its superior performance, is targeted to become the replacement for the MACH 4 family of devices.

Speedlocking™ for Guaranteed Fixed Timing

The ispMACH 4A architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed and SpeedLocking combine to give designs easy access to the performance required in today's designs.

Figure 2. ispMACH 4A Timing Model



Boundary Scan Testability

All ispMACH 4A devices have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

In-System Programmability (ISP™)

Programming devices in-system provides a number of significant benefits including rapid prototyping, lower inventory levels, higher quality and the ability to make field modifications. All ispMACH 4A devices provide In-System Programming capability through their Boundary Scan Test Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

ispMACH 4A devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO™ software facilitates in-system programming of ispMACH 4A devices. LatticePRO takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors used to drive the JTAG chain. LatticePRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program ispMACH 4A devices during board test.

PCI Compliant

ispMACH 4A devices in the -5/-55/-65/-7/-10/-12 speed grades are compliant with the PCI Local Bus Specification version 2.1, published by the PCI Special Interest Group (SIG). The 5V devices are fully PCI-compliant. The 3.3V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above VCC because of their 5V input tolerant feature.

Safe for Mixed Voltage System Designs

Both the 3.3V and 5V VCC ispMACH 4A devices are safe for mixed supply voltage system designs. The 5V devices will not overdrive 3.3V devices above the output voltage of 3.3V, while they accept inputs from other 3.3V devices. The 3.3V device will accept inputs up to 5.5V. Both the 5V and 3.3V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Pull-Up or Bus-Friendly Inputs and I/Os

All ispMACH 4A devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site at www.latticesemi.com.

All ispMACH 4A devices have a programmable bit that configures all inputs and I/Os with either pull-up or Bus-Friendly characteristics. If the device is configured in pull-up mode, all inputs and I/O pins are weakly pulled up. For the circuit diagram, please refer to *MACH Endurance Characteristics*.

Power Management

Each individual PAL block in ispMACH 4A devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

Programmable Slew Rate

Each ispMACH 4A device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3V/ns) or for the lower noise transition (1V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

Power-Up Reset/Set

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the VCC rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

Security Bit

A programmable security bit is provided on the ispMACH 4A devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

Hot Socketing

ispMACH 4A devices are well-suited for those applications that require hot socketing capability. Hot socketing a device requires that the device, when powered down, can tolerate active signals on the I/Os and inputs without being damaged. Additionally, it requires that the effects of the powered-down MACH devices be minimal on active signals.