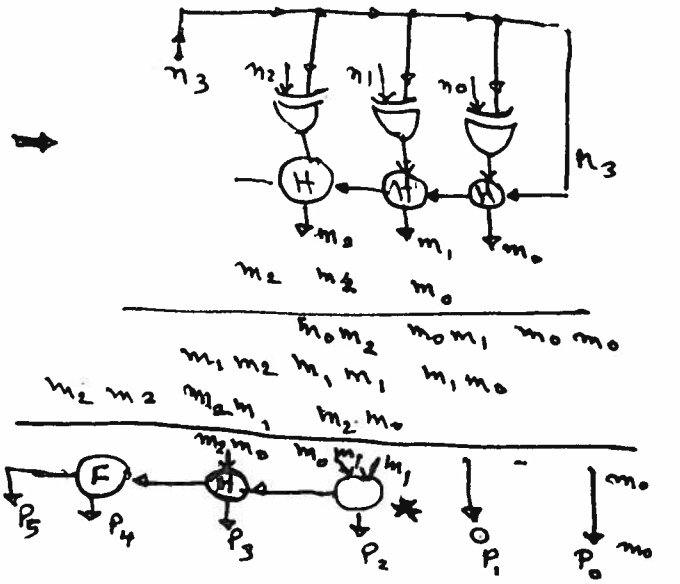
Question 1

Change $n_3 n_2 n_1 n_0$ Singed number to $m_2 m_1 m_0$



a)  for N^2

b)  for N^2+4

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Question 2

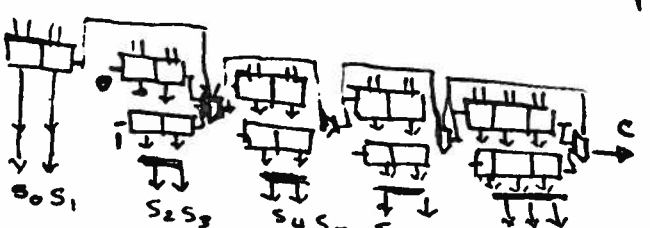
a) Selecting the breakdown of the 11 bit adder with minimizing delay as objective.

Options

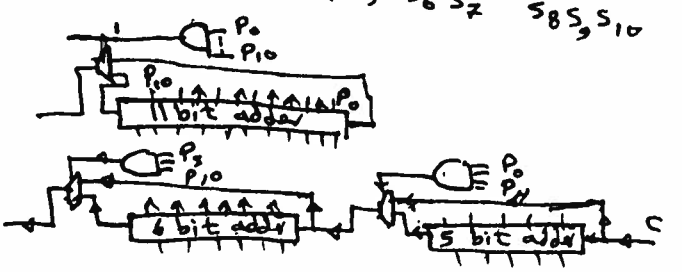
1) 2 2 | 2 | 2 | 3 | ---- 4δ ✓
2) 2 3 | 3 | 3 | ---- 4½ δ
3) 2 2 | 3 | 4 | ---- 4½ δ
4) 3 4 | 4 | ---- 5 δ
5) 1 1 | 1 | 2 | 2 | 2 | 2 | ---- 4 δ ✓

Since delay minimization is the objective Option-1 or 5 are both optimum so we look for optimum area within option 1 & 5

option 1) (5 + 9) MUX + 20 FA
option 2) (6 + 10) MUX + 21 FA } ✓



b)



The best scenario in term of delay is using 11 bit Ripple adder + MUX + AND but an AND of 11 inputs is not practical, so break down the adder to 5 & 6 Adder, each stage adds delay of MUX and AND gate.
So the Carry Select Adder is faster.

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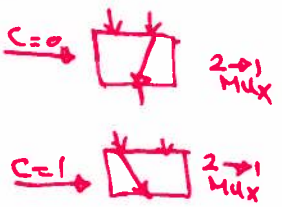
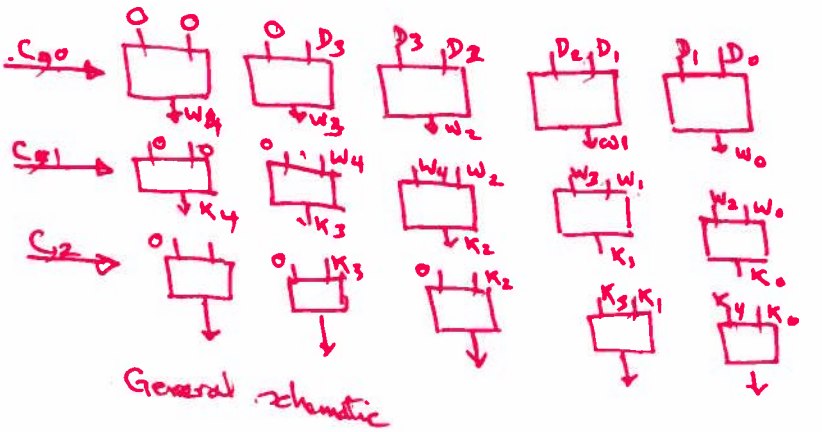
Q3

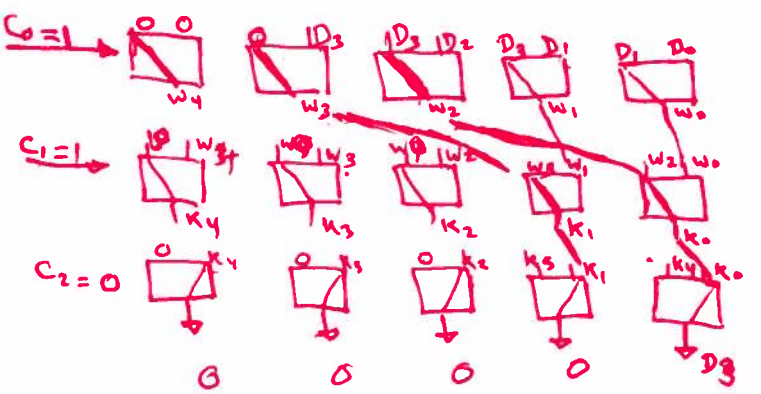
a) Both shift registers and barrel shifters are used for shifting data right or left. Barrel shifters shift several bits at the same time. Shift registers shift one bit at a time.
For the same amount of shifts barrel shifters are faster than shift registers but have large areas.

b)





General schematic



shifted output 000D_3

c) There is $\log_2^n$ = 3 rows of muxes so the delay of 3 shifts = delay of 5 shifts = $3\tau_m$