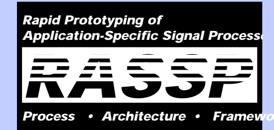
RASSP Design For Test Training



ATL Facility

March 28, 1996

8:00-11:30 AM

8:00-8:30	**Introduction**	**Tarzaiski**
8:30-9:15	**DFT Methodology**	**Sedmak**
9:15-9:45	**Test Architecture**	**Evans**
9:45-10:00	**Break**	
10:00-10:45	**Methodology Example**	**Tarzaiski**
10:45-11:15	**DFT Tools & String Example**	**Evans/ Sharma**
11:15-11:30	**Summary & Feedback**	**Tarzaiski**

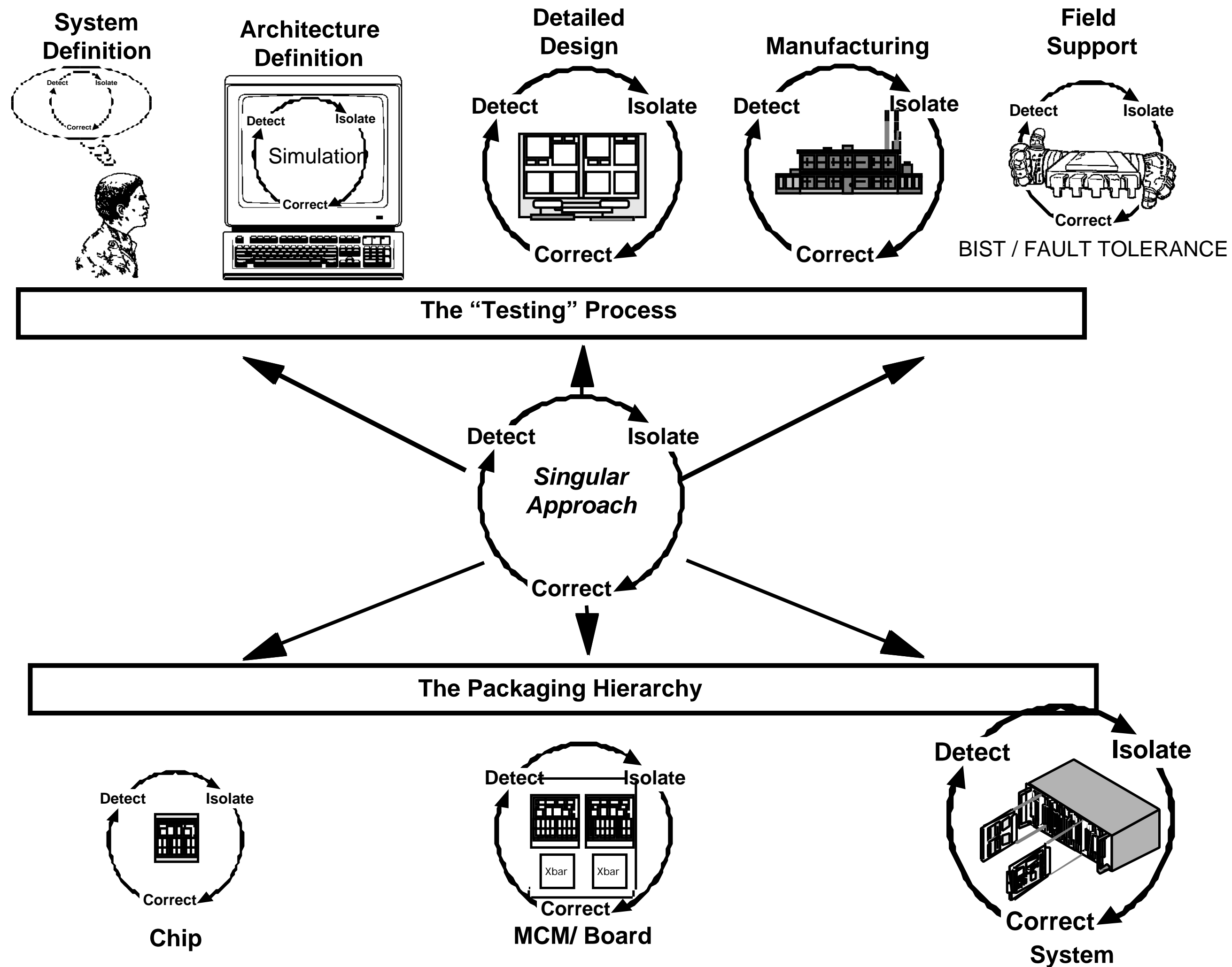
Design For Testability

- Incorporation of a Capability in any or all embodiments of a system
  - From requirements specification to simulation models to physical hardware and software
- Facilitates (in the case of DFT) or assimilates (in the case of BIST) test processes
  - Detecting, isolating, and possibly correcting anomalies
    - Design flaws, manufacturing defects, field defects
    - Anomalies may arise from any life cycle stage.
- Should be invocable at any stage of the life cycle.

DFT Methodology

- Terms and Definitions
- Overview of the DFT Methodology (2)
- Rel of Test Requirements, Test Strategies & Test Architecture
- Test Requirement Template
- Anatomy of a TSD
- Hierarchy of TSD's
- TSD Examples (6)
- DFT Reuse
- Test Domain Analysis

Expanded Definition of "Test"



•Singular Test Approach to achieve 4X.

Defect to Error Hierarchy

- **DESIGN FLAW: A mistake in the design of a circuit.**
- **DEFECT: A physical breakdown of an interconnection or device which represents a deviation from its specified requirements**
- **FAILURE: Incorrect transistor-level behavior, due to a defect**
- **FAULT: Incorrect gate level behavior, due to a failure**
- **ERROR: Incorrect circuit level behavior, due to the effects of a design flaw or the propagation of a fault through at least one level of gating.**

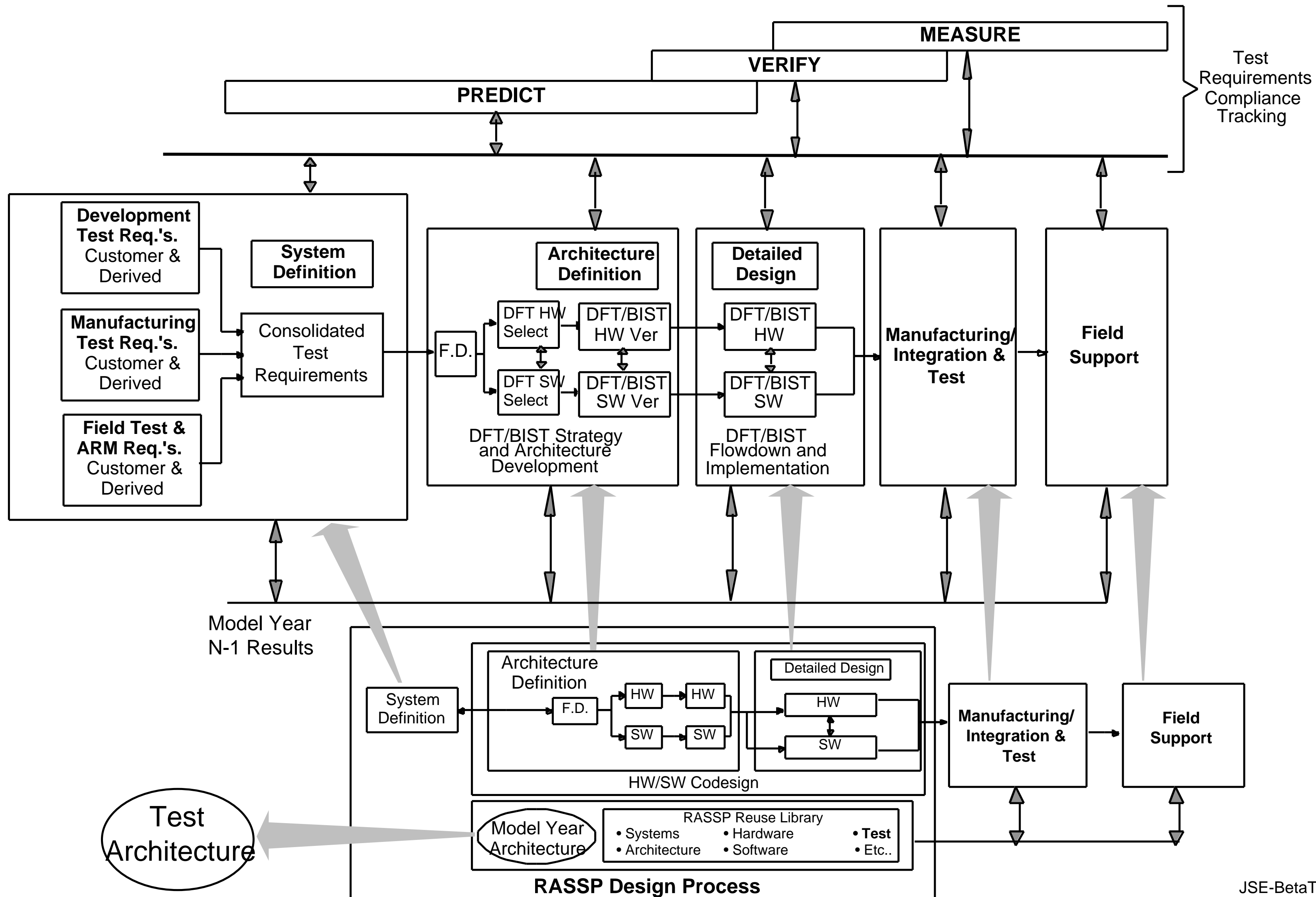
P/V/M & Metrics

- **PREDICTION: The assessment of the degree of compliance to test requirements through analysis or comparison with similar library elements.**
  - —Examples of means: Circuit level testability measures, topological dependency models
- **VERIFICATION: The assessment of the degree of compliance to test requirements through simulation or closed form proof.**
  - —Examples of means: Deterministic fault simulation, exhaustive test coverage proofs
- **MEASUREMENT: The assessment of the degree of compliance to test requirements through monitoring test performance on a physical item under test**
  - —Examples of means: automatic fault history logging, ATE-based data collection
- **METRICS: Quantitative parameters used for requirements specification, compliance tracking, and tradeoff analysis and selection**
- **TMAT: The Test Metrics/Tool Application Table, used in the Methodology to select a metric and a tool(s) or method to predict, verify, or measure compliance.**

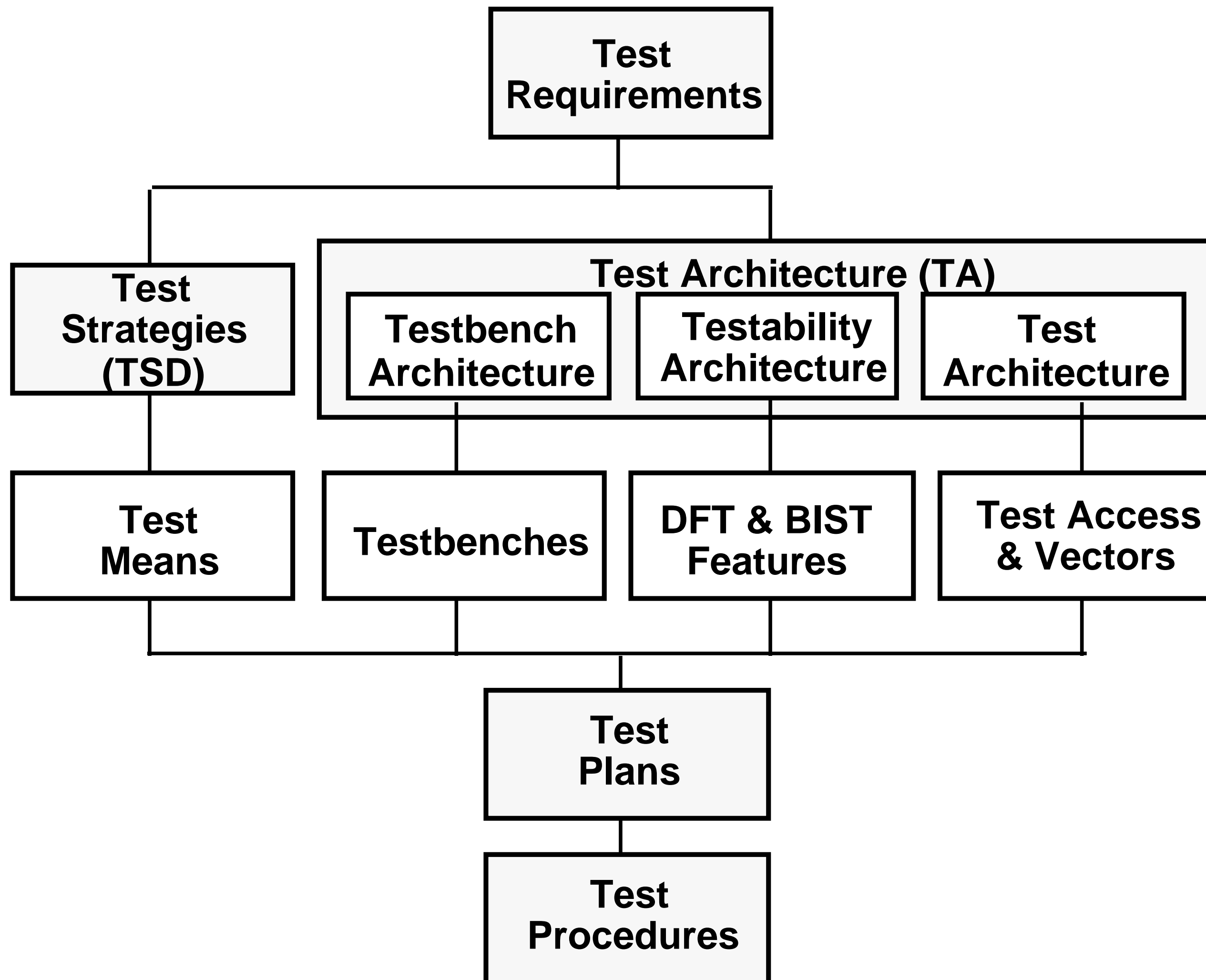
DFT Steps within Methodology (‘DFT Methodology’)

- Synthesis of ‘Top Down’ DFT process into overall RASSP methodology
- Requirements derived for all phases of Life Cycle Test (design, manufacturing and field)
- Flow down of test requirements, test architecture and strategies which span chip to system (Hierarchical)
- Emphasizes re-use in all dimensions
  - System Hierarchy
  - Life Cycle
  - Model years and future systems
- Reflects real World
  - Accommodate COTS at any level in the hierarchy
  - Accommodate refinement of test requirements and/or approaches as the development progresses
- Requirements conformance checking
  - Predict
  - Verify
  - Measure
- Designed to be
  - Implemented by tools within the RASSP timeframe
  - Accommodate different tool instantiations (e.g. Mentor or Cadence)
  - Extensible as new tools and architectures/methodologies are developed

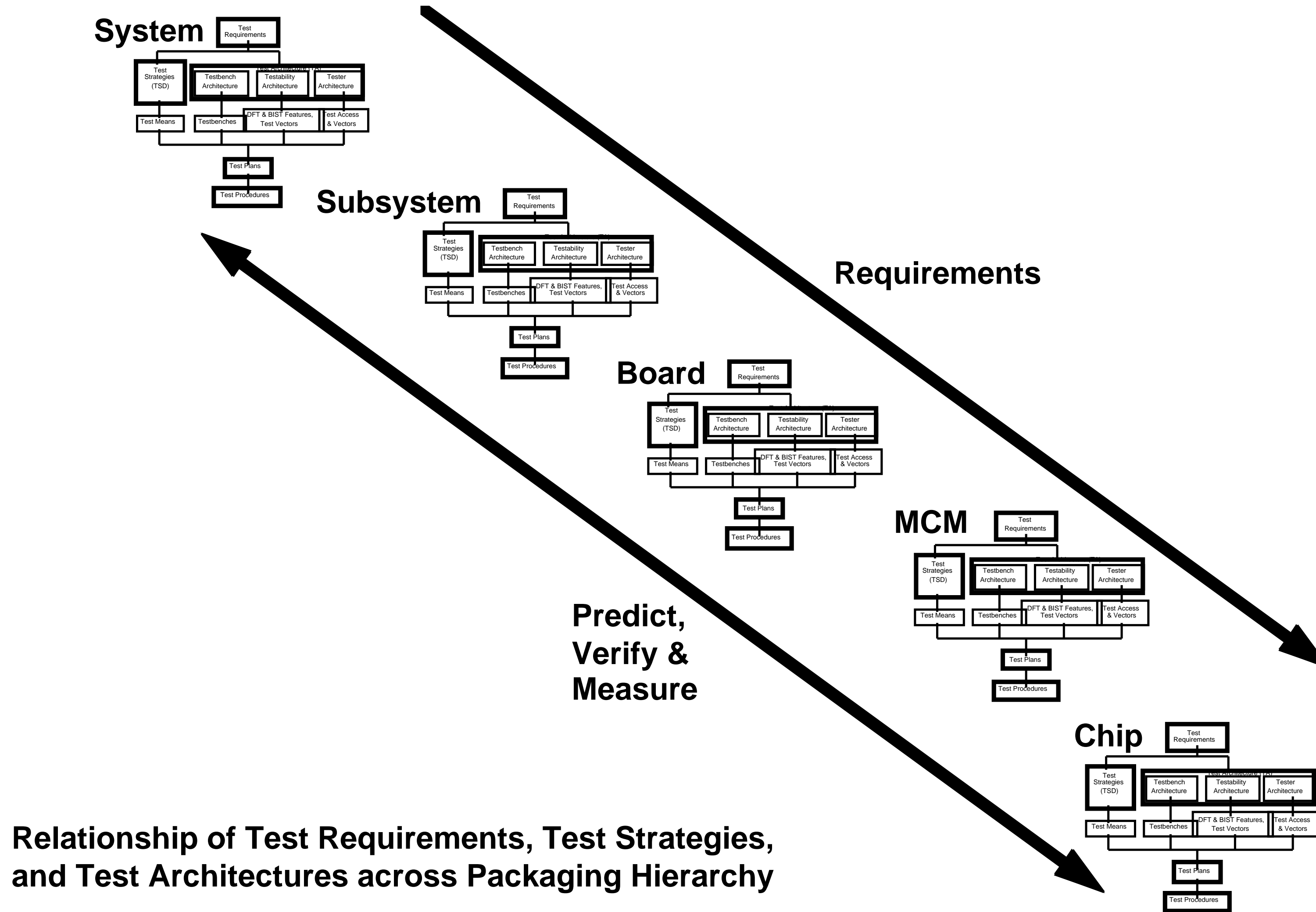
RASSP DFT Methodology in the Overall Methodology



Relationship of Test Requirements, Test Strategies and Test Architectures



Compliance Tracking



Relationship of Test Requirements, Test Strategies, and Test Architectures across Packaging Hierarchy

Test Requirement Template

- a. Test Phase
  - Design (e.g., simulation, prototype debug, qualification test, etc.)
  - Production (e.g., go/no test, diagnostic test, repair verification, etc.)
  - Field (e.g., operational, organizational, intermediate, depot)
- b. Test Means
  - BIST
  - Test Equipment
  - Manual procedures
  - Mix of above
- c. Test Mode
  - Power-on test
  - On-line concurrent (including interfering vs. non-interfering)
  - On-line non-concurrent (including periodic vs. event-driven, operator invoked or software invoked)
  - Off-line
- d. Degree of Allowable External Support
  - Operator may be "in the loop" to help achieve requirement
  - Troubleshooter may be "in the loop" to help achieve requirement
  - Job performance aid may be used to help achieve requirement

e. Fault Model Assumption

The definition of a "fault." For example, single stuck-at fault, multiple stuck-at fault, delay fault, intermittent fault, transient fault, etc.

f. Quantitative Definition of Metric

An equation defining the metric. For example, fault detection coverage might be defined as the total number of faults detected automatically by BIST, divided by the number of possible faults, with "fault" defined by the fault model above.

g. Prediction and Validation Weighing Factors

The factors used to allocate the requirements and later, to calculate system values from lower level values. For example, failure rate, usage rate, mission criticality etc.

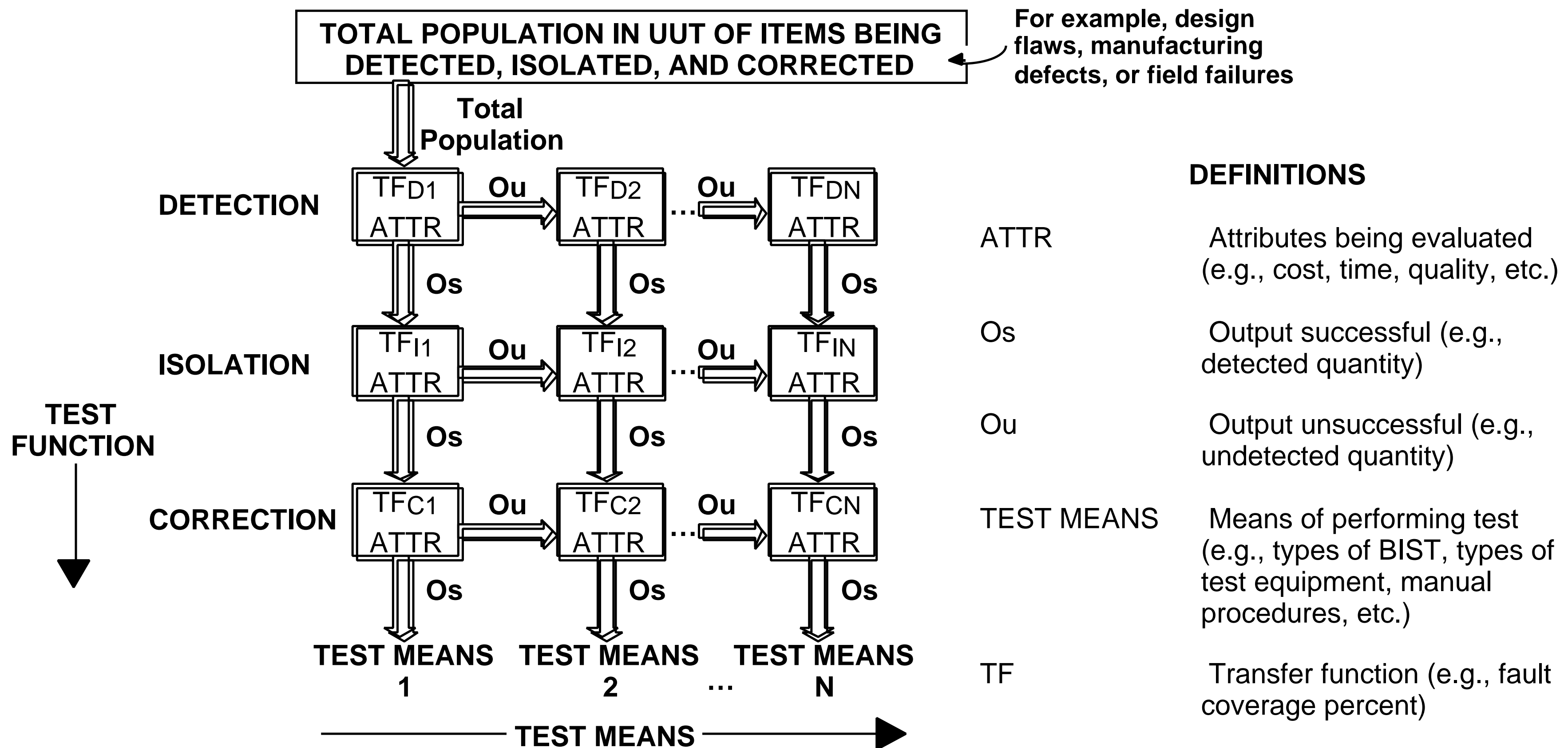
h. Quantitative Requirement

The actual quantitative requirement, calculated by the "quantitative definition" above. For example "98%."

i. Allowable Requirement Compliance Tracking Methodologies

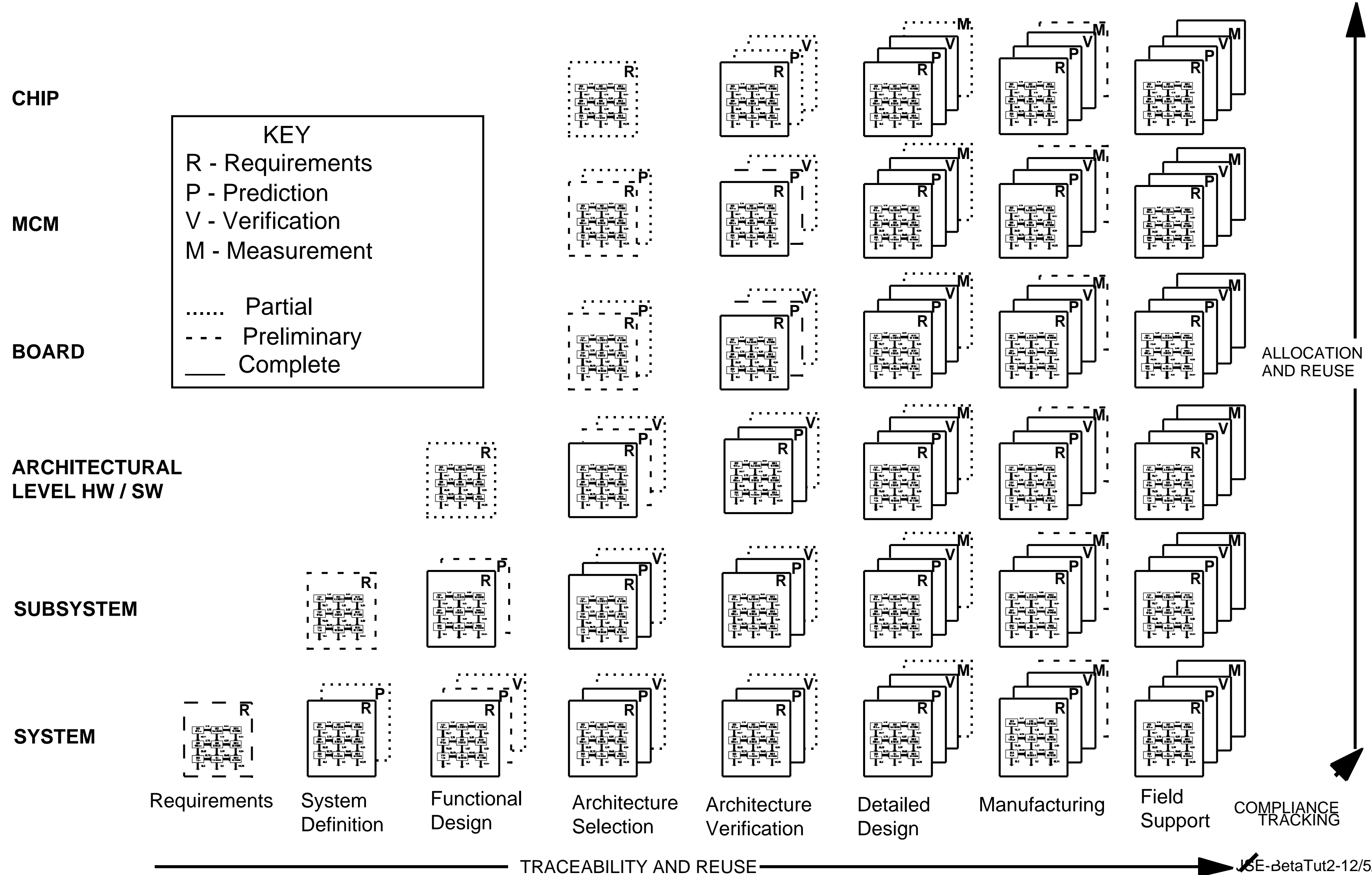
The means that may be used to track compliance to the requirement throughout the life cycle of the system. For example, topological dependency models at the prediction stage, fault simulation at the validation stage, and instrumentation or automatic fault-history logging at the measurement stage.

Anatomy of a Test Strategy Diagram

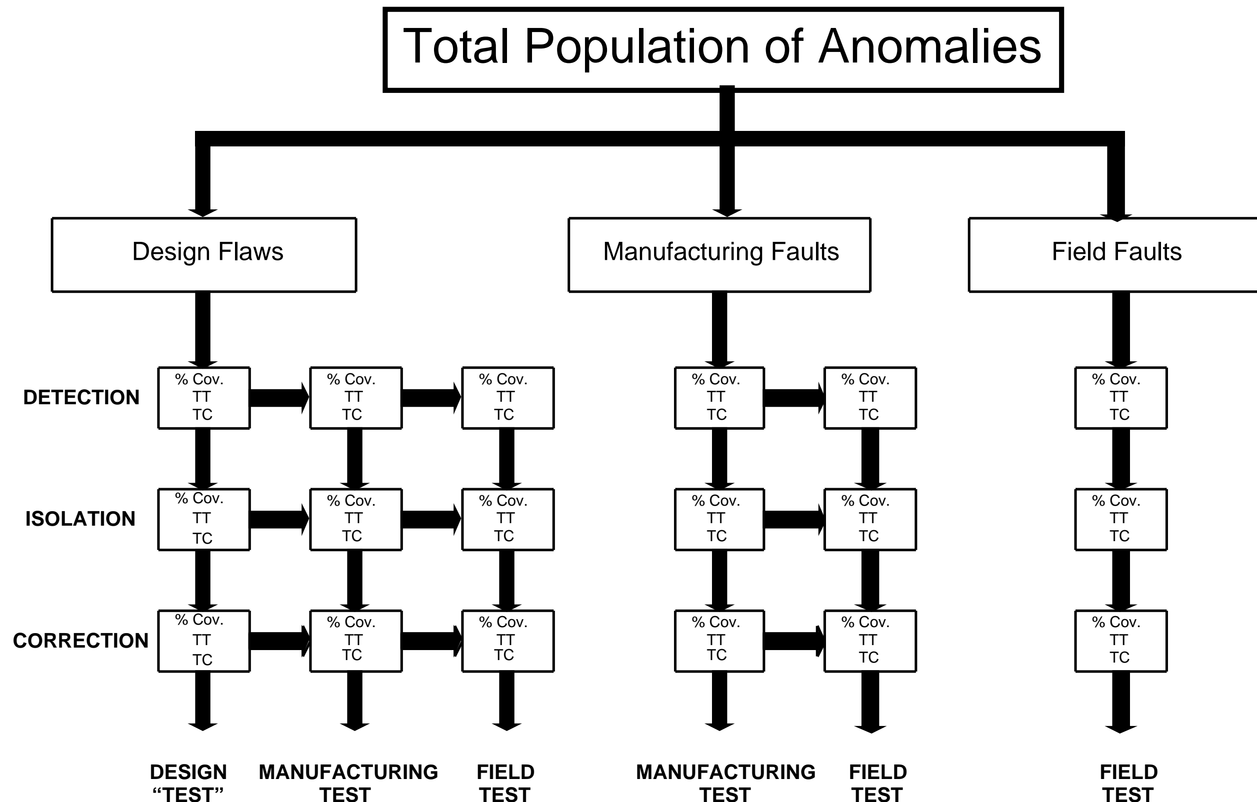


Key construct to bridge requirements to implementation, manufacturing and field support.

Hierarchy of Test Strategy Diagrams



TSD Example - Top Level



Example of a Top Level Test Strategy Diagram

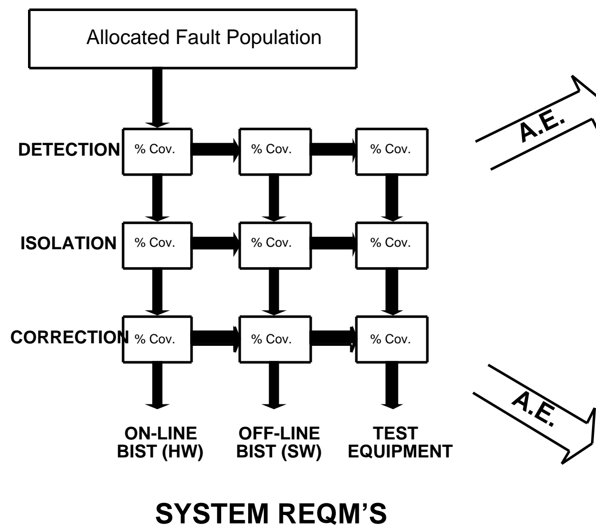
KEY

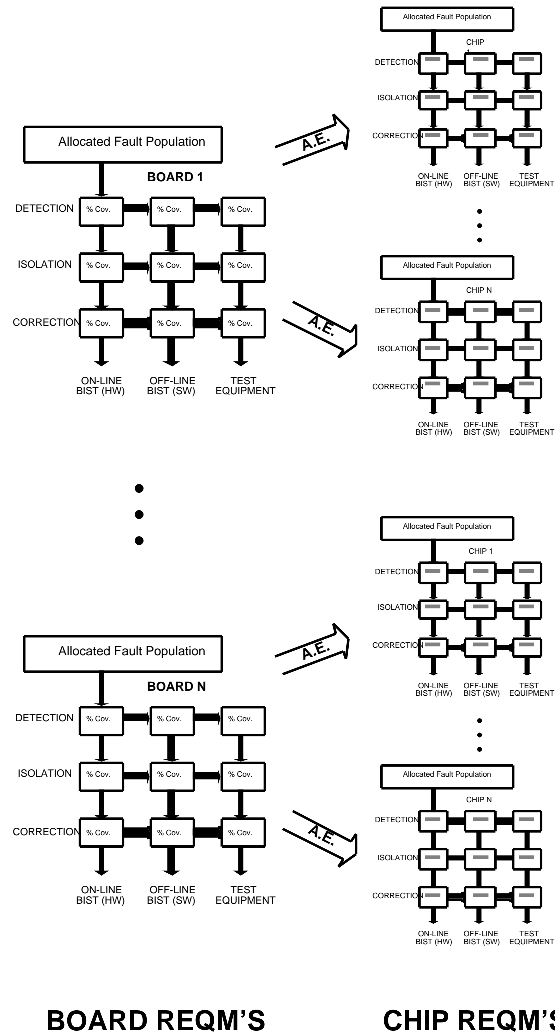
% Cov. - % Coverage
TT - Test Time
TC - Test Cost

TSD Example - BIST Allocation

KEY

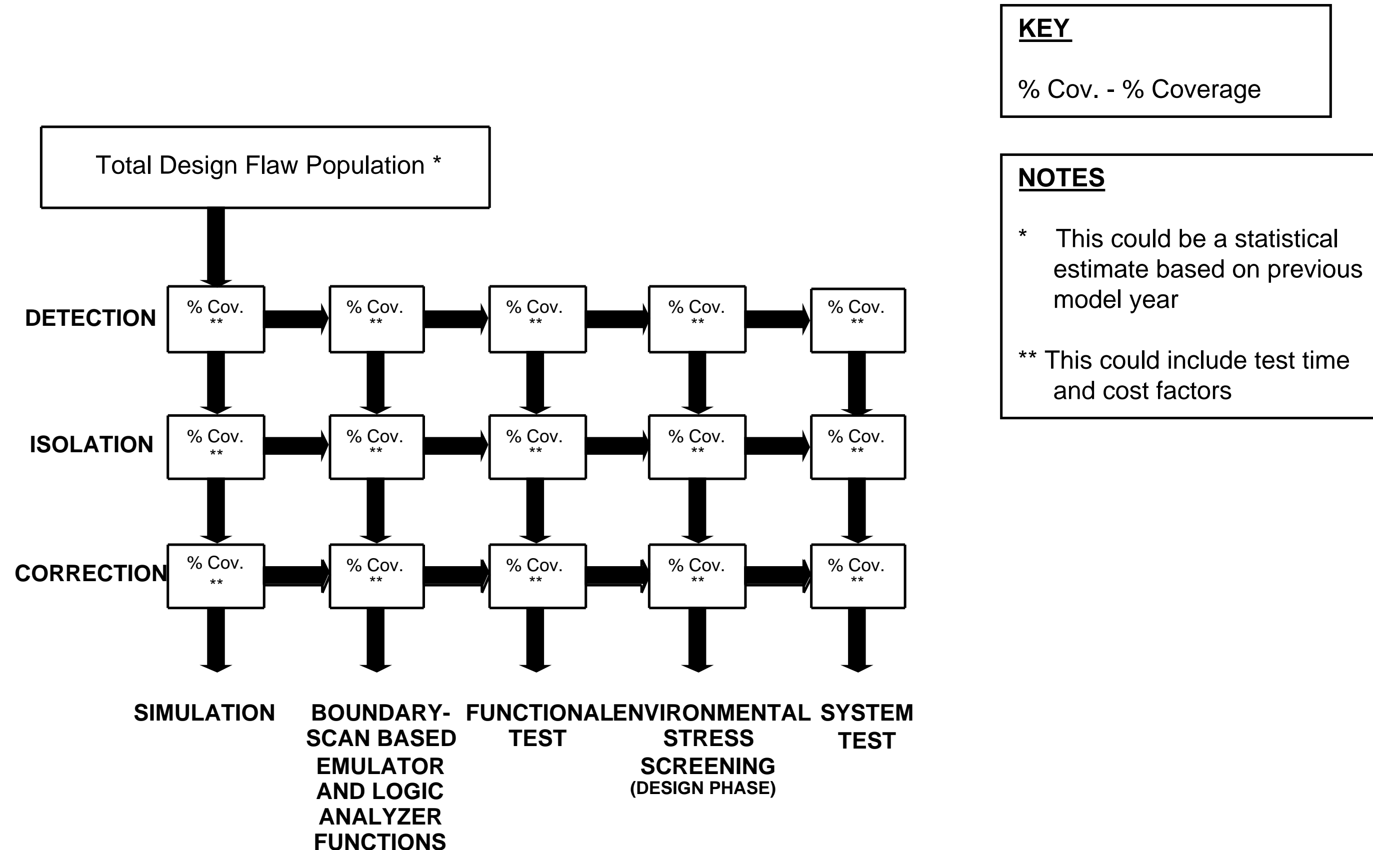
% Cov. - % Coverage
A.E. - Allocation Equation, based on factors such as failure rate, mission criticality, COTS versus Non-COTS, etc.





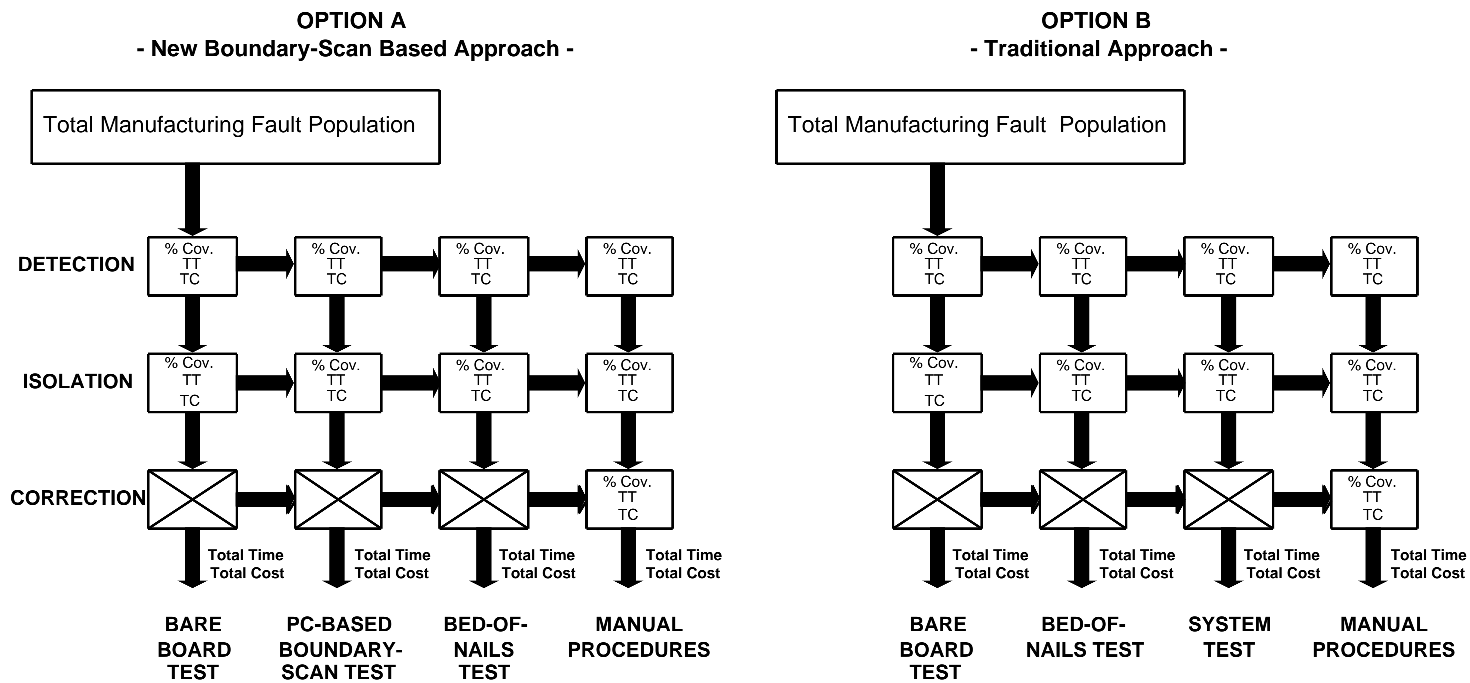
Example of a Test Strategy Diagram for BIST Requirements Allocation and Tradeoff Analysis for the Field Test Phase

TSD Example - Board Design Verification



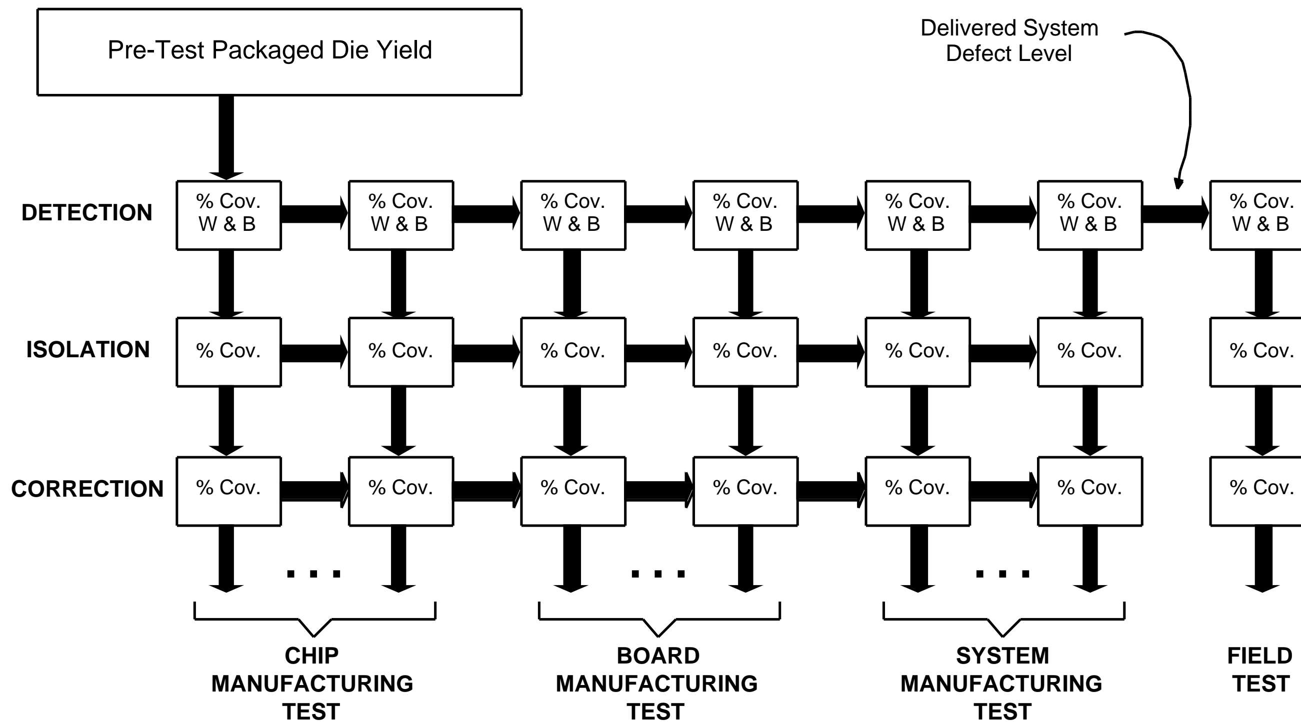
Example of a Board Level Test Strategy Diagram for Design Phase Test Strategy Development and Tradeoff Analysis

TSD Example - Board Test



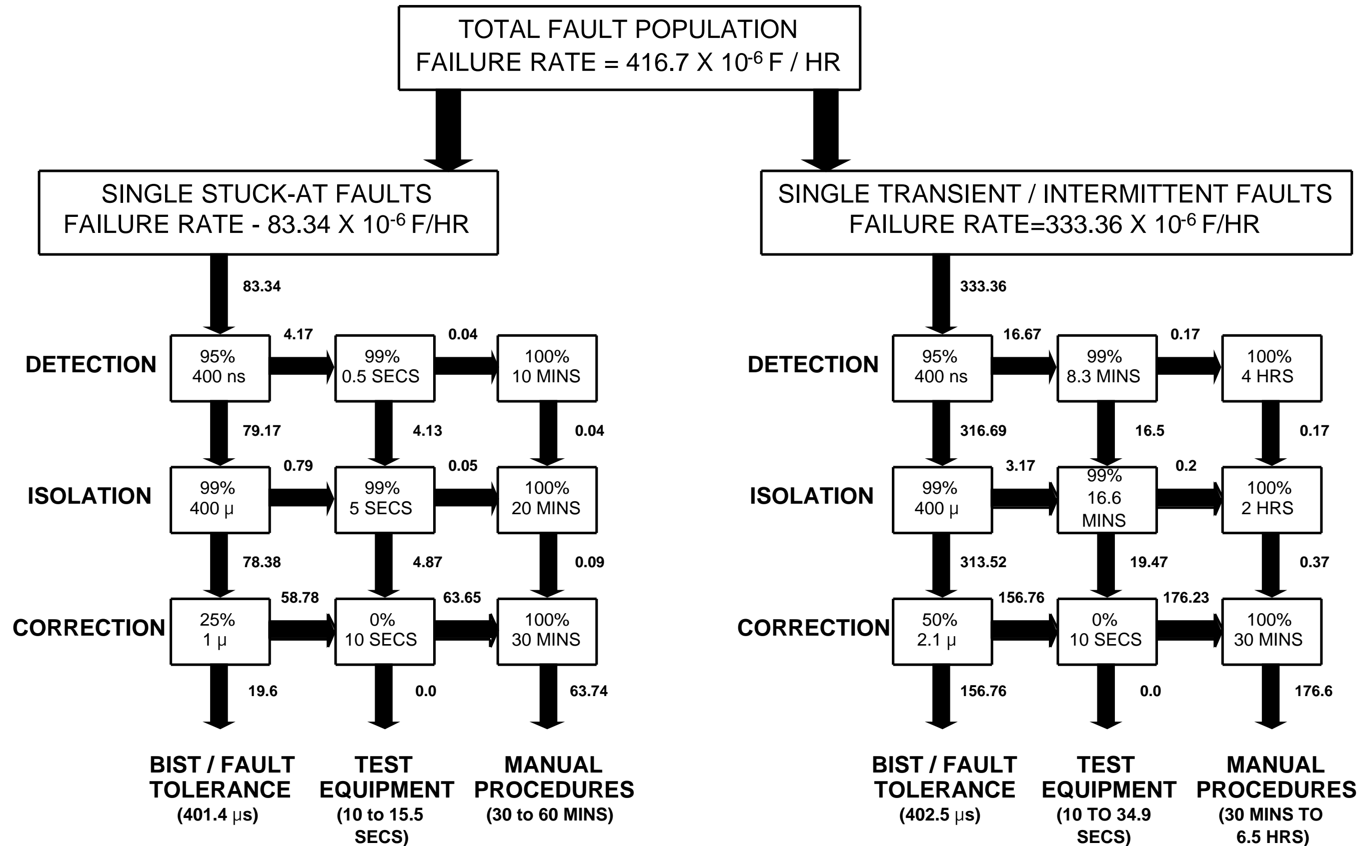
Example of a Test Strategy Diagram for Board Level Production Test Strategy Development and Tradeoffs

TSD Example - Defect Analysis



Example of a Test Strategy Diagram for Defect Level/Quality Level Analysis During Manufacturing

TSD Example - System Field Test



Example of a Test Strategy Diagram in the Field Test Phase for a System with BIST and Fault Tolerance

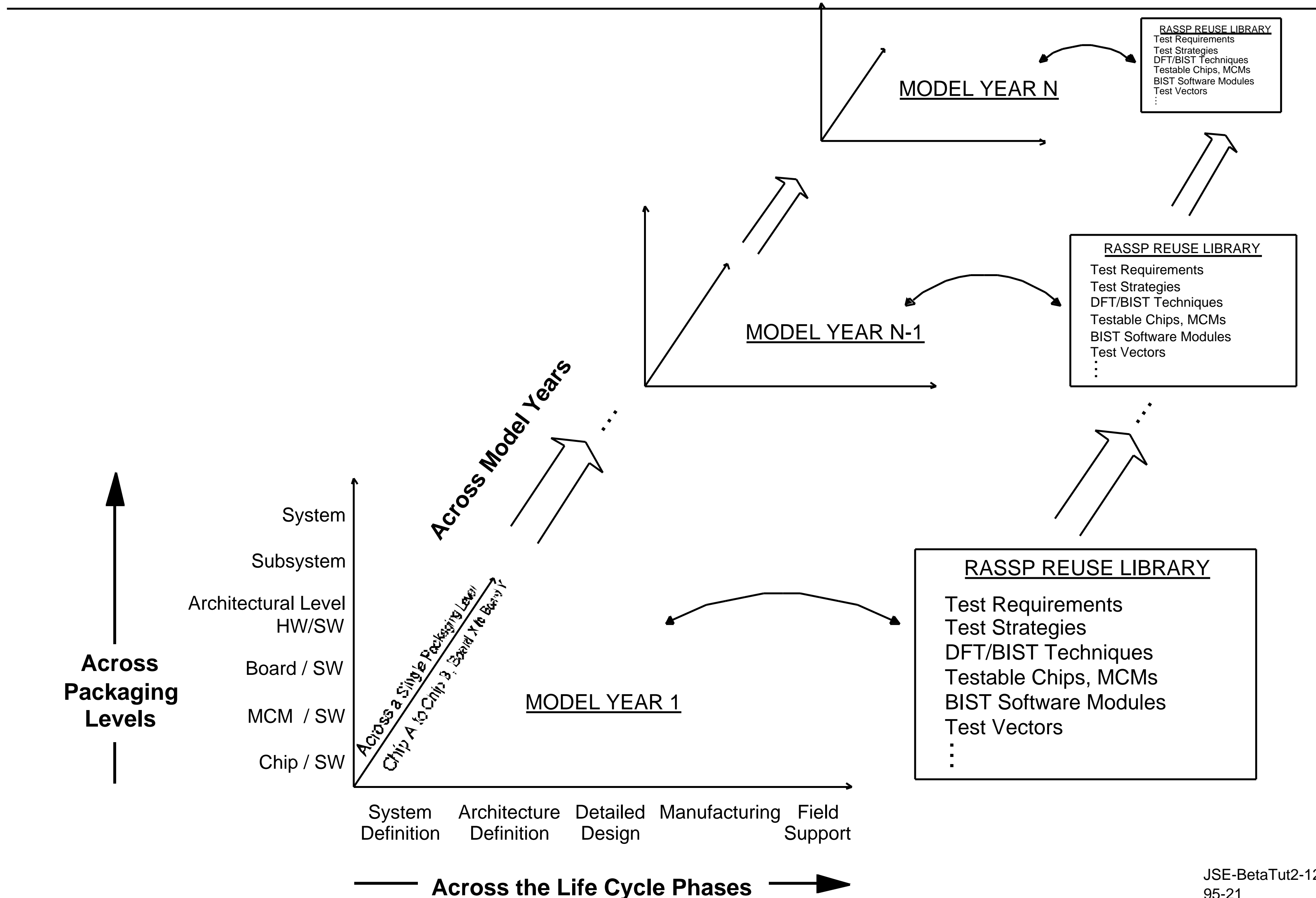
(Requirements Version)

NOTE:
The Correction Phase in the “Test Equipment” or “Manual Procedures” paths could also be handled by system level redundancy and reconfiguration.

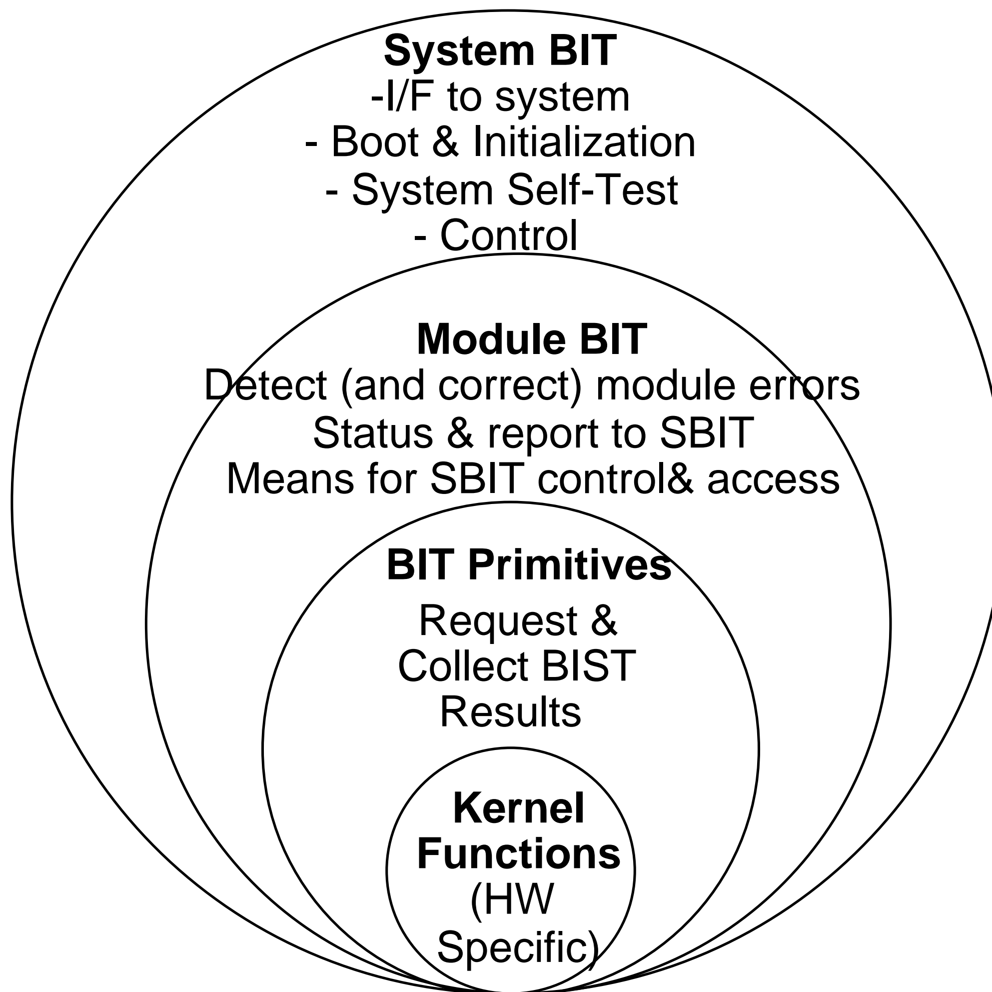
Reuse in the DFT Methodology

- **Reuse is the process of utilizing selected elements that are outputs from any process step from.....**
  - **earlier stages of the life cycle of a system**
  - **the same level of the system hierarchy**
  - **other levels of the system hierarchy**
  - **previous model years or previous systems**
- **Reuse contributes significantly to 4x improvement goal in the DFT and functional design processes.**
- **DFT itself is a major contributor to the 4x goal for the functional design process.**

Four Dimensions of Reuse in DFT



Reuseable BIST SW Vision



Re-useable CP's & DFG's.
Traceable to system spec.

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Traceable to system spec.

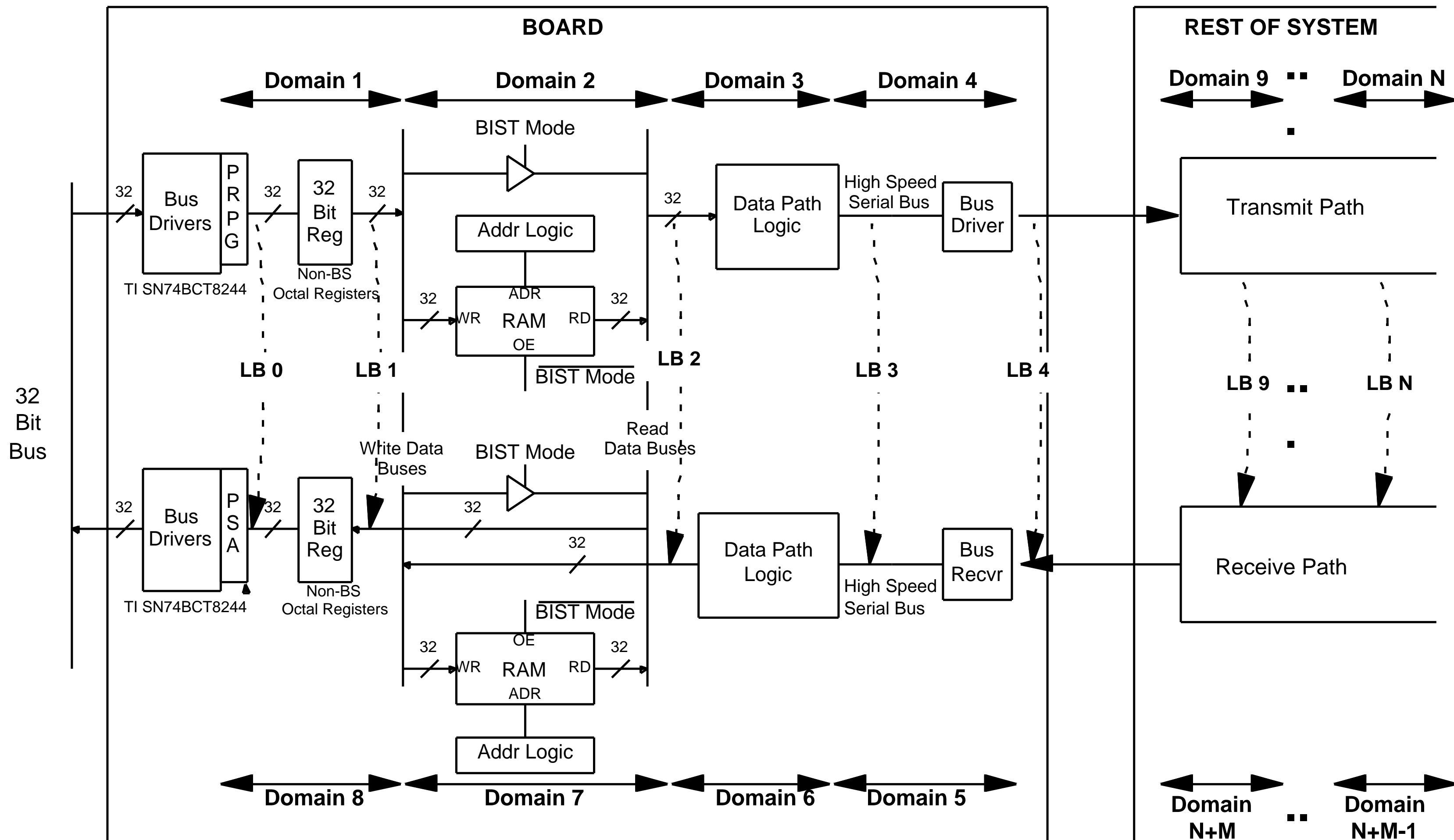
Re-useable primitive library
Forms **API/ Specifcation** for
lower level kernel functions.

Written to accomplish tasks &
provide results consistent with
BIT Primitive API.

Library Elements for Test Insertion and Development

- Templates for Test Requirements
- Example Test Strategy Diagrams for the three phases of test
- Templates of Test Plans & Procedures
- VHDL models of the T&M Architecture
  - Network architecture performance model
  - RTL capable of interacting with test SW such as ASSET (i.e. using LMG Smart Models for 8245's)
- Verfied BSDL/HSDL models of bscan components
- Re-useable BSCAN test fixtures &/or designs for MCA's & boards
- System BIST CP & DFG templates
- BIST 'Middleware" primitives (which provide interface specifications for low level BIST SW kernel developers)

Test Domain Analysis



Summary

- Methodology contributes significantly to achieving RASSP goals
- Methodology itself employs techniques for 4x improvement of DFT processes.
  - Reuse of test and BIST/DFT elements
  - Four dimensions of reuse
  - Life cycle employment of DFT/BIST
  - Use of automation where it exists
- Guided by, but not driven by, existing tools
- Expanded test and DFT definitions facilitate extensibility
- Test strategy diagrams help manage the DFT process
  - Are flexible and extensible