Beta Site Tutorial
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Tutorial on RASSP Design-For-Testability

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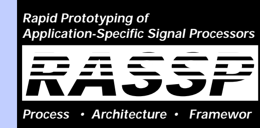
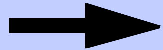
RASSP Design For Test Training



ATL Facility

March 28, 1996

8:00-11:30 AM



8:00-8:30	Introduction	Tarzaiski
8:30-9:15	DFT Methodology	Sedmak
9:15-9:45	Test Architecture	Evans
9:45-10:00	Break	
10:00-10:45	Methodology Example	Tarzaiski
10-45-11:15	DFT Tools & String Example	Evans/ Sharma
11:15-11:30	Summary & Feedback	Tarzaiski

Introduction

- Tutorial Objective and Scope
- Other DFT Tutorial Resources
- Who are DFT Methodology Users?
- The Test Problem
- The Design Test Problem
- The Manufacturing Test Problem
- The Field Test Problem
- The DFT Solution
- RASSP DFT Goals & Scope
- Integration of DFT into RASSP

Tutorial Objective and Scope

- Course Objective - Provide a top level view into the RASSP DFT developments & methodology.
- Hands-on example of key parts of the DFT Methodlogy (Test Requirements and Test Strategy Diagram).
- Demonstration of some tool “integrations” and application.
- IS NOT:
  - comprehensive
  - a primer on specific DFT techniques and tools
  - focused on chip level DFT

Other DFT Tutorial Resources

- “RASSP DFT Methodology Tutorial”, LM-ATL, R. Sedmak & J. Evans.
- ASSET, DFT & BIST Training Courses offered by Self-Test Services (R. Sedmak).
- “Test Technology Overview”, RASSP E&F, Dr. Robert H. Klenke, rhk2j@hal.ee.virginia.edu.
- Solution Strategies Workshops - “Test For ASIC’s” & “BSCAN DFT for ASIC, IC & Bd Design”, Mentor Graphics Corp. & Hewlett Packard.
- TI Testability CD-ROM, Testability Handbook, Boundary Scan Tutorial & ASSET Preview
- Teradyne Victory Preview Disk
- WAVES Web Site & CD ROM

Who are DFT Users?

- **Customer** — **Test Requirements , Test Strategies, Test Architectures,**
- **Design Engineer** — **Test Requirements, Test Strategies, Test Architectures, DFT Implementation**
- **Test Engineer** — **Test Requirements, Test Strategies, Test Architectures, DFT Implementation, Test Plans, Test Procedures, Test Programs**
- **Manufacturing** — **Test Requirements, Test Strategies, Test Equipment & Fixtures, Test Programs, Test Application, Data Collection**
- **Field** — **Test Requirements , Test Strategies, Test Programs, Test Fixtures, Test Application, Data Collection**

The Test Problem

- Growing complexity
  - Chip on System, 100 Mhz+ clocks
  - Chip Scale packaging
- Growing demand
  - explosion in semiconductor & electronics
- Reduced time to market
  - cellular phones & notebook computers have a 6 month product window
- Increased demand for quality
  - 6 Sigma
  - ISO 9000

The Design Test Problem

- **General Test Problem + ...**
  - **Multi-Processor Hardware / Software Integration**
    - **In-Circuit Emulation**
  - **Lack of models for complex, Off-The-Shelf (OTS) ASIC's, DSP's, Boards and Systems**
  - **Isolation of Design Flaws from Manufacturing Defects**

The Manufacturing Test Problem

- **General Test Problem + ...**
  - **Electronics being manufactured exceed capabilties of ATE**
  - **ATE costs increase while overall reliability is going down due to the number of channels and the complexity of each channel**
  - **Increased test time translates into less units out per day translates into more capacity required to meet demand**

The Field Test Problem

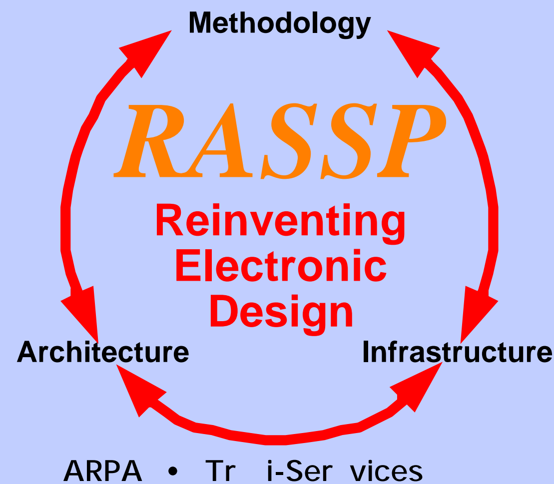
- General Test Problem + Manufacturing Test Problem + ...
  - Re-engineering Test Programs Sets for the ATE the depot has (vs the factory)
  - Logistics
    - Spares
    - Troubleshooter skill level
    - On-site vs remote dignostics
  - Keeping track of revisions/ ECO's in the field
    - Which version do I have?
    - Should I replace this unit?

The DFT Solution

- Singular Test Architecture (Design/ Manufacturing/ Field) reduces development effort by three
- Hierarchical, Independent Test & Maintenance architecture
- Built-In Self Test and Automatic Fault-History Logging
- Predictable, Verifiable and Measurable process for DFT development

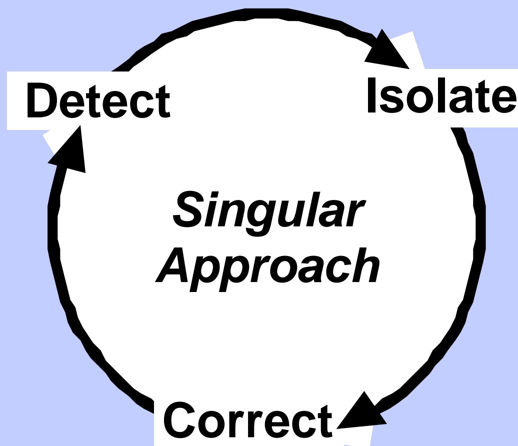
RASSP Program Objectives and Goals

- The objective of the Rapid Prototyping of Applications Specific Signal Processors (RASSP) program is to improve the process of designing, manufacturing, and fielding embedded digital signal processors
- Major goals
  - 4x reduction in time for initial design or upgrade
    - Commensurate improvements in quality, life cycle cost, and supportability
    - State-of-the-art when fielded
  - Commercialization and promulgation of the RASSP process



RASSP DFT METHODOLOGY GOALS

- **Hierarchical approach integrated with RASSP processes**
- **Support and facilitate RASSP goals**
- **Foster reuse of test and BIST/DFT elements**
- **Guided, but not driven, by existing tools**
- **Accommodate presence of COTS in the system**



RASSP Concepts which DFT Leverages

RASSP Concept	Benefit	DFT Leverage	Benefit
Model Year Architecture & Standard Virtual Interface	Low cost technology upgrades over model years and across products	Embed Testability Architecture into MYA	Facilitate singular test philosophy & ease of upgrades
Virtual prototype	Early verification of top down, Hierarchical model of system	Embed BIST resources into VP	Early test & debug of BIST functions
HW/SW Co-Design	Simpler integration & test & Improved product quality	Capture Testability Architecture in Performance Models & DFG's	Early development of test functions facilitates HW/SW Integration
Enterprise Infra-Structure	Automation and control of process and reuse of components and data	Embed DFT steps in workflows and re use libraries	Integration of DFT into RASSP

RASSP concepts provides a good framework for integrating design with test.

Benefits of Integrating DFT into RASSP

Approach	Benefit
1. Consolidate test requirements	1. Reduce overall test development efforts and cost
2. Incorporate TSD construct	2. Bridge requirements to implementation
3. Extend concept of re-use	3. Minimize impact of test on schedule and cost
4. Implement conformance checking (via TSD).	4. Consistent framework for feedback of model year results.
5. Model test resources in VP	5. Concurrent test development shortens schedule
6. Integrate test architecture with MYA	6. Consistent use; Model year upgrades of test resources

Design-For-Test Integration Tasks

- Work Flows and Activity Definitions
- DFT Tool Integration's
  - CAT or Test Specific (Fault simulation, Testability Analysis, DFT/ BIST insertion, ATPG, ...)
  - CAE or Re-use of functional engineering tools (HDL Entry, SW development, simulation, Data Management, ...)
- Re-use Libraries
  - Object Class Hierarchy (DOCH)
  - Contents of re-use elements (what data constitutes a re-use element)
  - Initial population of critical elements
- Templates and standards for test related product data
- Training
  - Benefits
  - Process
  - Tools