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**Developed by:** Qualis Design Corporation

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**DESCRIPTION:** Can't quite remember the proper syntax for a Verilog statement? Confused about which VHDL conversion functions are supported in Synopsys' STD\_LOGIC\_ARITH package? No problem. Just download these Quick Reference Cards and the entire language syntax will be right at your fingertips.

You can also receive these QRCs on 2-sided, tri-folded, incredibly durable paper direct from Qualis. Really. Just send us your request via [e-mail](#).

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