PinEditor v5.0 User's Guide

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Introduction

Welcome to PinEditor

The PinEditor tool provides a graphical application for displaying and configuring I/O assignments and attributes.

Use PinEditor to:

- assign I/O macros to pins
- fix pin assignments that have automatically been assigned during layout
- view and print pin assignments
- assign I/O standards to banks, for families that utilize I/O banks
- edit I/O attributes, such as I/O standards, slew, and capacitance
- assign VREF pins, for I/O standards that require an input reference voltage

To start PinEditor:

There are three ways to start PinEditor:

- Click **PinEditor** in the Designer main flow window
- From the **Tool** menu, click **PinEditor**
- Click the **PinEditor** toolbar button in Designer

PinEditor Interface

Package window

PinEditor's Package window displays pins, I/O macro assignments, and I/O Banks (Axcelerator family only).

The Package window is integrated with PinEditor windows and list boxes. If you select an assigned pin in the Package window, the pin location is highlighted in the World View window and the I/O macro name is selected in the Assigned list box and the I/O Attribute Editor.
The Package Window displays detailed information about each pin, including:

- pin number
- special pin properties, such as JTAG, clock, ground, or power
- assigned I/O macro name, if any
- pin type, represented by color

Color Manager

Use the Color Manager to customize the colors used to display the package in ChipEditor and PinEditor. The Color Manager specifies the display colors for I/O banks, I/O FIFO Blocks, RAM tiles, Core tiles, clusters, super clusters, and nets.

To customize the colors in the Package window:

1. From the **View** menu, click **Color Manager**.
2. In the Color Manager dialog box, click the color box in front of the item you wish to customize, or click the I/O bank you wish to change. The color pallet is displayed.
3. Select a color and click **OK**. The new color will appear in the Color Manager dialog box.
4. After you are done customizing your colors using the Color Manger dialog box, click **OK**.

World View window

The World View window's default location is under the Assigned list box. Use the World View window to control which portion of the package is displayed in the Package window. The blue rectangle (known as the Package rectangle) represents the package. The green rectangle (known as the Viewing rectangle) represents the currently displayed area in the Package window.
To display another part of the package, use the left mouse button to drag the Viewing rectangle to the area on the Package rectangle you would like to display. To specify a new display area, use the right mouse button to stroke out a new Viewing rectangle on the Package rectangle.

I/O Attribute Editor

The default location of the I/O Attribute Editor is below the Package and World View windows. The I/O Attribute Editor lists all assigned and unassigned I/O macros and their attributes in a spreadsheet format. Use the I/O Attribute Editor to view, sort, select, and edit these I/O attributes. Double-click a column heading to sort by that attribute. If you select a macro in the list boxes, the I/O attribute editor scrolls to highlight the selected macro.

Configure PinEditor List Boxes

Use the Configure List Box dialog box to customize what is displayed in the Assigned and Unassigned list boxes.

To configure the listboxes:

1. From the **View** menu, click **Configure List Boxes.**

2. **Filter Assigned and Unassigned Lists**: Entering a specific pin name in this field filters out all other pins in the Assigned and Unassigned List Boxes. Use the * wildcard to filter for groups.

3. **Show fixed and unfixed pins**: Selecting this causes all fixed and unfixed pins to be displayed in the Assigned list box.

4. **Show only fixed pins**: Selecting this filters out all unfixed pins from the Assigned list box.

5. **Show only unfixed pins**: Selecting this filters out all fixed pins from the Assigned list box.

2. Click **Apply** to see changes. When satisfied, click **OK**.

Making Pin Assignments

Use PinEditor to make and edit I/O macro pin assignments. Edits made in PinEditor are permanent, as long as they are fixed and committed.

Depending upon the design family, PinEditor opens as a stand alone tool or in the MultiView Navigator.

To assign an I/O macro to a pin using PinEditor in the MultiView Navigator interface:

1. Select the instance in the Logical or Physical tabs.
2. Drag the instance to the pin location.

   If the location is a valid one, the macro is assigned and automatically fixed.

To assign an I/O macro to a pin using stand alone PinEditor:

1. Select the macro name in the Unassigned list box. The macro is simultaneously selected in the I/O Attribute Editor.
2. Assign the selected macro to a pin location using any one of these methods:
   - Drag the selected macro name from the Unassigned list box to the pin location in the Package Window. Valid pin locations are highlighted in the Package Window.
   - In the Edit menu, choose **Assign** to invoke the Assign mode. Then, select the pin location in the Package Window.
   - Click the **Assign** toolbar button to invoke the Assign mode and then select the pin location in the Package window.
   - If you know the specific pin location, enter the pin assignment in the Pin# cell or select a valid placement from the drop-down menu.

If the location is a valid one, the macro is assigned and automatically fixed. The status bar displays information about invalid assignments. Choose *Extended Error Messages* from the Help menu for more information about specific error messages.

Note:

- If you assign a macro to a pin that has already been assigned a macro, the previously assigned macro becomes unassigned, even if its placement has been fixed.

Locking Pin Assignments

Designer does not alter locked pins during Layout. Designer recognizes pins as locked if they are:

- assigned manually using PinEditor
- assigned in a design schematic
- assigned using a pin file (non-Axcelerator ProASIC families)
- assigned using a PDC file (Axcelerator family only)

Locked pins are permanent, as long as you commit your locked pins to your design before you exit PinEditor.

To lock pins:

1. Select the pin(s) to lock in the Assigned list box, Package window, or I/O Attribute Editor. To select multiple pins, hold the ctrl key and select multiple pins with your mouse. To select all pins, choose **Select All** from the **Edit** menu.
2. In the **Edit** menu, click **Lock**. Or, using the I/O Attribute Editor, select the Locked check box.

Note:

- If you are using the I/O Attribute Editor, you can only fix one pin at a time.

To unlock a pin:

1. Select the pin(s) to unlock in the Assigned list box, Package window, or I/O Attribute Editor. To select multiple pins, hold the ctrl key and select multiple pins with your mouse. To select all pins, choose **Select All** from the **Edit** menu.
2. In the **Edit** menu, **click Unlock**. Or, in the I/O Attribute editor, uncheck the Locked check box.

Closing and committing pin assignments

Edits made in PinEditor are only temporary. If you wish to keep your pin assignments and I/O attribute changes, you must commit your changes before closing PinEditor.

To commit your pin assignments at any time, from the **File** menu, click **Commit**.

To commit your pin assignments when closing PinEditor click Yes when asked if you would like to commit changes made in PinEditor.

Committing your changes saves them to the "working" design for this Designer session only.

To permanently save changes made in PinEditor to your design file, (.adb) you must save your design. From the Designer **File** menu, click **Save**.

Configuring I/O Banks (Axcelerator Family)

About I/O Banks

For devices that support multiple I/O standards, I/Os are grouped onto I/O banks around the chip.

The Axcelerator Family has 8 I/O banks that surround the chip, two per-side, numbering 0-7. The I/O banks are color coded for quick identification. (Colors can be changed using the Color Manager.)
Each I/O bank has a common:

- VCCI, the supply voltage for its I/Os
- VREF, the reference voltage bus (for voltage-referenced I/O standards)

Only one VREF value can be assigned to each I/O bank. Only I/Os compatible with both the same VCCI and VREF standards can be assigned to the same bank.

Assigning technologies to I/O Banks

To assign technologies to banks:

1. Select an I/O bank.
2. From the **Edit** menu, click **I/O Bank Properties**.
3. In the Configure I/O Dialog Box, select your options and click **Apply**. The I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are removed.
4. If VREF pins can be assigned, the Assign VREF Pins button will highlight.

5. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.
6. Click **OK**. Using PinEditor, proceed to assign I/Os with the same standards to the appropriate banks.

I/O Bank options

When assigning technologies to your I/O banks, use the Configure I/O Bank dialog box.

Options include:

Select Technologies

Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Further selecting GTL (3.3V) disables SSTL3 as an option because the VREFs of the two are not the same.

Assign VREF Pins

After you have selected your technology, click Apply. If VREF pins are required, this button becomes activated. Click to assign VREF pins. You must assign VREF pins at least once.

Click More Attributes to set the following:

Low Power Mode (Optional)

Select Enable Input Buffers or Enable Output Buffers. These are not required. This feature is not supported in the RTAX-S family.

Input Delay

Drag the slider bar to your desired delay. The delay is bank specific. Drag the meter to your desired delay index. The delay code and typical value appear. Click **View All Delays** to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall) for the input delay selected. A

technology must be selected in order to see the input delays. Click **OK** to dismiss the View All Delays dialog box. This feature is not supported in the RTAX-S family.

Specifying I/O bank voltage

You can directly specify voltages for each I/O bank by doing one of the following:

- Using the Assign Technologies to I/O Banks dialog box
- Placing an I/O of a particular technology in an I/O bank that has not been assigned a voltage
- Using the command set_iobank in a PDC File

Using the I/O Attribute Editor

About the I/O Attribute Editor

The I/O Attribute Editor displays I/O attributes in a spreadsheet format. Use the I/O Attribute Editor to view, sort, select, and edit standard and device-specific I/O attributes.

I/O Attributes

Standard attributes

The I/O Attribute Editor shows four standard attributes for all I/O macros:

- **Port Name** indicates the I/O macro name.
- **Macro Cell** indicates the type of I/O macro.
- **Pin #** indicates the current pin assignment.
- **Fixed**, if checked, indicates that you cannot change the current pin assignment during layout.

Axcelerator I/O attributes

Besides the standard attributes, the I/O Attribute Editor displays Axcelerator specific attributes. The list below includes a description of Axcelerator specific attributes.

1. **I/O Standard** indicates the I/O standard. Possible I/O standards include LVTTL, LVCMOS 2.5V, LVCMOS 1.8V, LVCMOS 1.5V, 3.3V PCI, LVDS, LVPECL, GTL+, HSTL Class I, SSTL3 Class I and II, and SSTL2 Class I and II. Information on these standards can be found in "Glossary" on page 51. Refer to the appropriate data sheet for information about I/O standards for different families.
2. **Slew** indicates the slew rate for output buffers. Generally, available slew rates are high and low. The output buffer has a programmable slew rate for both high to low and low to high transitions. The slow slew rate is incompatible with 3.3V PCI requirements. For the Axcelerator family, slew can only be edited for the LVTTL I/O standard.
3. **Resistor Pull** indicates the resistor pull: NONE, weak pull-up, Weak pull-down. The default value is NONE. The only exception to this is an I/O that exists in the netlist as

a port, is not connected to the core, and is configured as an Output Buffer. In that case, the default setting will be for a weak pull-down.

4. **Hot Swap** indicates if the pin is hot swappable. The device, the
5. **I/O standard** specified, and the selected voltage determine this read-only attribute. All the I/O standards except 3.3V PCI are hot-swap compatible and 3.3V tolerant.
6. **Loading** (pf) indicates the output-capacitance value based on the I/O standard selected in the I/O Standard cell.
7. **Input Delay** is set to "on" by checking the box.
8. **Output Drive** Strength can be set to 8, 12, 16, 24 in mA, weakest to strongest. The LVTTL output buffer has four programmable settings of its drive strength. Other I/O standards have full strength.
9. **Bank Name** displays the bank name. This cannot be edited.

SX-A and RTSX-S I/O Attributes

Besides the standard I/O attributes, the I/O Attribute Editor displays device-specific attributes. Device-specific attributes vary by device and only supported attributes are displayed. The list below includes a description of SX-A and RTSX-S specific attributes.

1. **I/O Standard** indicates the I/O standard. Possible I/O standards include LVTTL/TTL, PCI, CMOS, Custom. Information on these standards can be found in "Glossary" on page 51. Refer to the appropriate data sheet for information about I/O standards for different families.
2. **IO Threshold** indicates compatible threshold level for inputs and outputs, either CMOS, TTL, or PCI.
3. **Slew** indicates the slew rate for output buffers. Generally, available slew rates are high and low. The output buffer has a programmable slew rate for both high to low and low to high transitions. The slow slew rate is incompatible with 3.3V PCI requirements.
4. **Resistor Pull** indicates the resistor pull at power-up time: NONE, weak pull-up, Weak pull-down. This state is of short duration and does not stay. The default value is NONE. The only exception to this is an I/O that exists in the netlist as a port, is not connected to the core, and is configured as an Output Buffer. In that case, the default setting will be for a weak pull-down.

5. **Hot Swap** indicates if the pin is hot swappable. The device, the I/O standard specified, and the selected voltage determine this read-only attribute. All the I/O standards except 3.3V PCI are hot swap compatible and 5V tolerant.
6. **Loading** (pf) indicates the output-capacitance value based on the I/O standard selected in the I/O Standard cell. If you have selected custom in the I/O Standard field, you can modify the capacitance value to any integer value that accurately reflects the capacitive loading on the Actel device pins.

ProASIC and ProASIC PLUS I/O Attributes

Besides standard I/O attributes. the I/O Attribute Editor also displays device-specific attributes. Device-specific attributes vary by device and only supported attributes are displayed. The list below includes a description of ProASIC ProASIC PLUS and specific attributes.

1. Loading (pf) indicates the output-capacitance value based on the I/O standard in the I/O Standard cell. The loading selected is applied to all outputs.

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