Actel Tools®:Timer

User's Guide

R1-2003

Windows® and UNIX® Environments

Actel

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Trademarks

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Introduction

Timer is Actel's static timing analysis tool. Timing simulation is a convenient and thorough method of analyzing, debugging and validating the timing performance of a design. This is achieved by breaking down the design into sets of paths. Delays for each path are then calculated and every path is checked for timing violations.

Unlike dynamic timing analysis, static timing analysis does not require vectors. This enables static timing analysis tools to run faster and accommodate larger designs. Complex functions are easier to analyze using the static analysis because it offers one hundred percent coverage with minimal effort.

The Actel Timer tool does not check the functionality of a design, and timing simulation may be more suited for asynchronous parts of a design and is required for any mixed-signal portions. For timing simulation of your design, use the Backannotate function to back annotate post-layout delays to your CAE simulator.

Actel Timer comes in two flavors. The first type includes SX-A, eX, AX, and ProASIC families. The first flavor uses the "pin-to-pin timing model," since Timer reports a pin-to-pin delay on these devices. The second flavor uses the "input-to-input" timing model, and applies to all other families. For families that use the input-to-input timing model, delays are reported from an input gate to the input of the next gate by lumping gate and net delays together. Not all the features described in this manual are available for all devices. Minor exceptions for device families are noted in the text.

Document Organization

This guide provides detailed cross-platform information about Timer. Use it as a reference in your everyday work.

It provides step-by-step instructions for Windows and Unix platforms. Platform differences in procedures and commands are noted in the text.

This user's guide is divided into the following chapters:

Chapter 1 - Getting Started with Timer introduces Timer's graphical user interface and menu commands.

Chapter 2 - Using Timer contains information on how to use Timer to analyze timing performance and set timing constraints.

Appendix A - Using Keywords describes how to use keywords to create custom sets.

Appendix B - Glossary defines key terms used in this guide.

Appendix C - Product Support provides information about contacting Actel for customer and technical support.

Document Assumptions

The information in this manual is based on the following assumptions:

1. You have installed the Designer Series software.
2. You are familiar with UNIX workstations and UNIX operating systems, or with PCs and Windows operating environments.
3. You are familiar with FPGA architecture and FPGA design software.

Document Conventions

The following conventions are used throughout this manual.

Information that is meant to be input by the user is formatted as follows:

```
keyboard input
```

The contents of a file is formatted as follows:

```
file contents
```

Your Comments

Actel Corporation strives to produce the highest quality online help and printed documentation. We want to help you learn about our products, so you can get your work done quickly. We welcome your feedback about this guide and our online help. Please send your comments to **documentation@actel.com**.

Actel Manuals

Designer and Libero include printed and online manuals. The online manuals are in PDF format and available from Libero and Designer's Start Menus and on the CD-ROM. From the Start menu choose:

- Programs > Libero 2.3 > Libero 2.3 Documentation.
- Programs > Designer Series > R1-2003 Documentation

Also, the online manuals are in PDF format on the CD-ROM in the "/manuals" directory. These manuals are also installed onto your system when you install the Designer software. To view the online manuals, you must install Adobe® Acrobat Reader® from the CD-ROM.

A complete list of the the Designer Series documents is available on the Actel website at http://www.actel.com.

Online Help

The Designer Series software comes with online help. Online help specific to each software tool is available in Libero, Designer, ACTgen, ACTmap, Silicon Expert, Silicon Explorer II, and Silicon Sculptor.

1

Getting Started with Timer

This chapter contains details about Timer's user interface and commands. For information on using Timer to perform static timing analysis please refer to "Using Timer" on page 21.

Enter and save constraints using Timer before running Timing Driven Layout for timing critical designs. Also, importing timing constraint files forces Timer to use Timing Driven Layout.

Invoking Timer

You can only use Timer after you open a compiled design (*.adb file), or after compiling a netlist in designer. If you invoke Timer before compiling your netlist, Designer guides you through the compile.

There are three ways to invoke Timer:

1. Choose Timer from the Tools menu, or
2. Click the Timer icon in Designer's toolbar, or

3. Click the Timer button in Designer's design flow.

Timer opens in a separate window, as shown in Figure 1-1 on page 10.

Timer

Timer's four tab screens organize and display static timing information according to the timing analysis preferences you set in the Preferences dialog box (see "Setting Preferences" on page 35.)

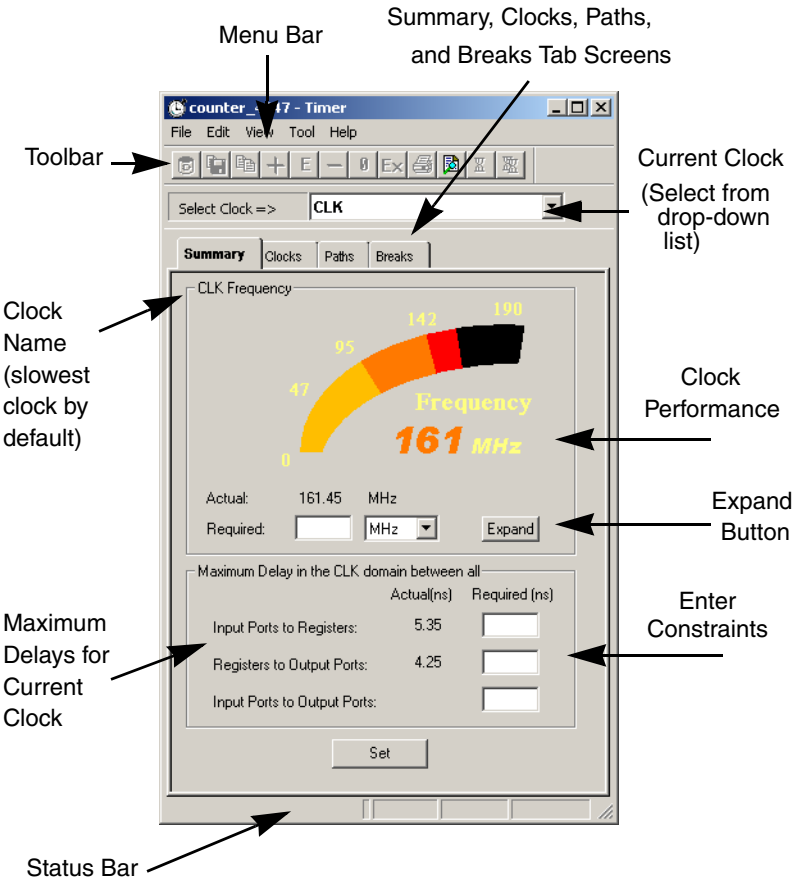

Figure 1-1. Timer Summary Tab Screen (PC only)

Timer consists of four tab screens: Summary, Clocks, Paths, and Breaks. Each of these tab screens is described below.

Note: Timer does not display the Clocks tab screen if the design you are analyzing has no clock.

Summary Tab

By default, Timer's Summary tab screen, as shown in Figure 1-1, displays the maximum frequency for the current clock selected in the current clock drop-down list box.

Note: UNIX does not display the speedometer graphic representing the clock performance.

To change the default clock, select from the drop-down clock list next to the toolbar.

Click the Expand button to show the details of the path that determined the max clock frequency.

Displayed in the lower portion is the actual longest/shortest delay in the clock domain between all:

- Input ports to registers
- Registers to output ports
- Input ports to output ports

Enter timing constraints in the Required control boxes next to each category.

IMPORTANT: By adding constraints to the set of paths listed in this tab, be careful that you do not over-constrain the design. This may degrade the quality of the Timing Driven Layout and increase the overall run time.

Clocks Tab

The Clocks tab, as seen in Figure 1-2, allows you to enter constraint information and set clock exceptions. You can also set your default clock in the Clock Selection toolbar.

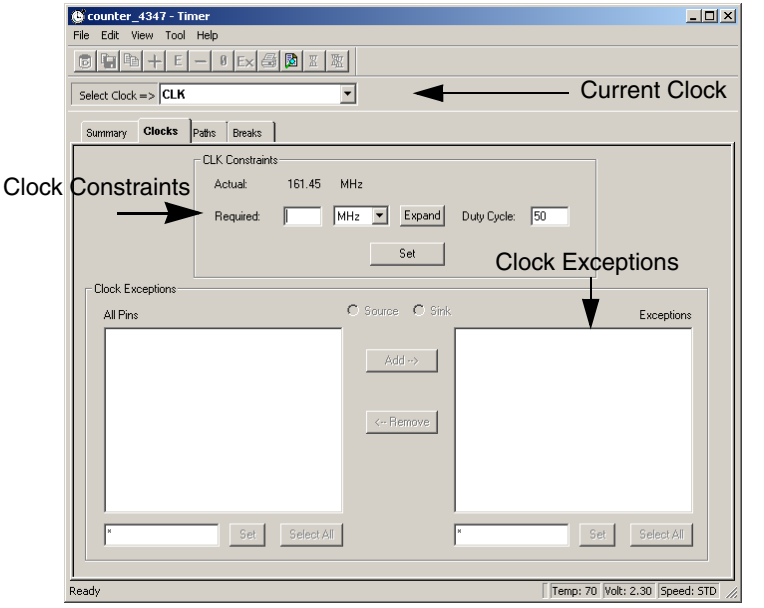

Figure 1-2. Clock Tab

Enter constraint information in the Constraints area and click Set.

Clock exceptions are terminals in a synchronous network that should be excluded from the specified clock analysis (see "Clock Exceptions" on page 42).

Paths Tab

The Paths tab, as shown in Figure 1-3, displays timing analysis information for categories of paths, known as "sets," and the paths within each set. The pre-defined sets are shown below. The Paths tab displays the sets in an upper grid and the paths within each set below.

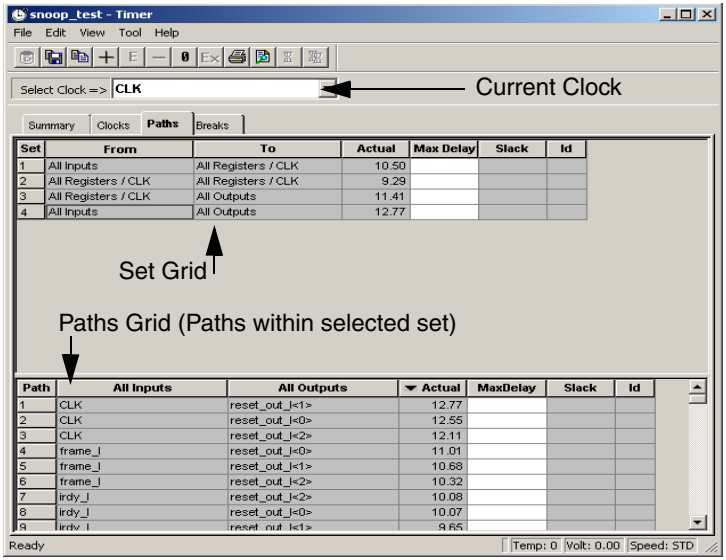

Figure 1-3. Paths Tab

The Paths tab default setting displays four path sets:

- **From All Inputs TO All Registers / CLK:** All paths from the input ports of the design to the input pins of all the registers in the current clock domain. In this instance, CLK is an example of the current clock domain.
- **From All Registers / CLK TO All Registers / CLK:** All paths from the clock pin of registers in the current clock domain to the input pins of all the registers in the current clock domain; in this instance, CLK is an example of the current clock domain.[1] To view the register setup and clock skew, right-click the desired path in the paths grid and select Expand Path from the shortcut menu.

1. *Applies only to families that use the pin-to-pin timing model.*

- **From All Registers / CLK TO All Outputs:** All paths from the clock pin of registers in the current clock domain to the primary outputs of the design.
- **All Inputs TO All Outputs:** All input ports to all output ports in the design. This set is completely asynchronous (independent of the clock).

All the sets default to display the longest path in the category. You can change this default setting by selecting Preferences from the File menu.

When you select a set, Timer displays the paths within the set in the lower spreadsheet labelled "Paths." The spreadsheet displays a sorted list of paths (the number of paths it displays is controlled in the Preferences dialog box). Double-click the column headings to sort the columns.

Note: The run-time required to compute the content of the spreadsheet is a function of the number of paths you wish to display. Select Preferences from the File menu to change the default settings.

The timing information displayed for sets and paths includes:

- **Actual:** The actual delay calculated by Timer for each path.
- **Slack:** The difference between the maximum required delay and the actual delay.
- **Max Delay:** The maximum required delay specified. Do not interpret this value as the clock frequency. To set clock frequency, input on the Summary tab, or on the Clocks tab (Figure 1-1 and Figure 1-2, respectively).
- **ID:** The constraint ID for the path.

Breaks Tab

The Breaks tab screen (Figure 1-4) is used to enter global stops and pass pins. A global stop is a defined intermediate point in a network that forces all paths through the defined point to be "don't care" paths regardless of any constraint assignment Setting a pass pin on a module pin will allow you to see a path

through individual pins, which you are not normally allowed to view a path through.

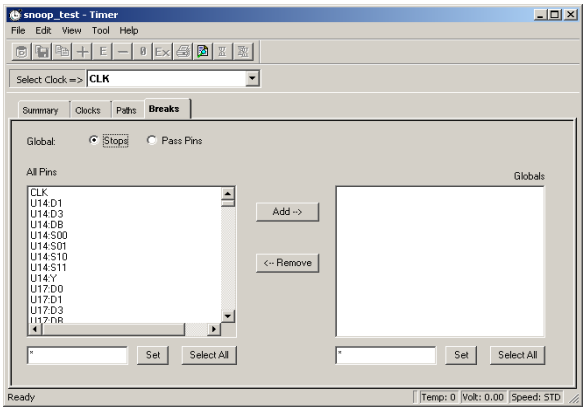

Figure 1-4. Breaks Tab

Timer Toolbar

The Timer toolbar (Figure 1-5) contains commands for performing common Timer operations on your designs. Click on a button in the toolbar to access a command.

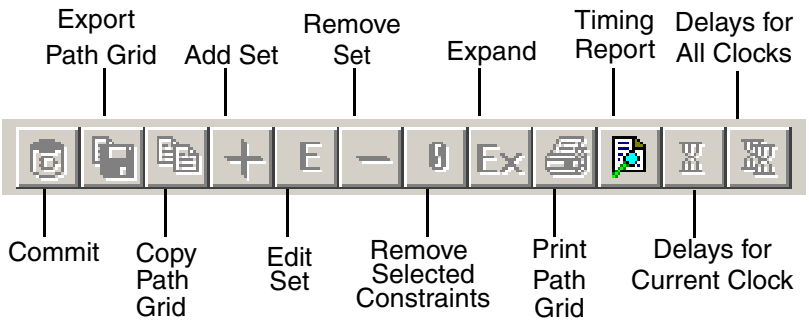

Figure 1-5. Timer Toolbar

Timer Menu Commands

The PC and workstation versions of Timer have the same menus. However, some dialog boxes may look slightly different on the two platforms due to the different window environments. The functionality is the same on both platforms, though the locations of the fields and buttons on the dialog boxes may vary. The names of some fields may also vary between the PC and workstation versions.

File Menu

Commit: Commits Timing information to Designer

Export Set Grid: Exports selected cells in the sets grid to a file

Export Path Grid: Exports selected cells in the path grid to a file

Print Set Grid: Prints selected cells in the sets grid

Print Path Grid: Prints selected cells in the paths grid

Operating Conditions: Displays the operating conditions Timer uses to calculate delays

Preferences: Invokes Preferences dialog box, where you can set analysis and display preferences

Close: Closes Timer

Edit Menu

Copy Set Grid: Copies set grid to clipboard

Copy Path Grid: Copies path grid to clipboard

Remove Selected Constraints: Removes selected constraints, not all

Remove All Constraints: Removes all constraints in Timer

Expand Paths: Expands path in new window

Add Set of Paths: Defines and adds new path set to Paths tab

Edit Set of Paths: Edit added path set

Remove Set of Paths: Removes added path sets

Tool Menu

Report Paths: Generates Timing report

Report Violations: Generates a Timing report, timing violations only

Calculate delays: Calculates delays for the current clock

Calculate all delays: Calculates delays for all clocks and selects the worst (clock with greatest delay)

Help Menu

Help Topics: Lists of Help Topics

Reference Manuals: Opens Timer's User's Guide

Status Bar

Timer's status bar, located at the bottom of Timer's window, displays information on menu commands and error messages. In addition, Timer displays the following:

1. **Temp.** Displays the temperature consistent with the operating conditions selected.
2. **Volt.** Displays the voltage consistent with the operating conditions selected.
3. **Speed Grade.** The speed grade of the selected device.

Calculating Delays with Timer

The way that Timer reports timing information varies depending on the device family you are using. For ACT1, ACT2 (for ACT 2 and 1200XL devices), ACT3, 3200DX, 40MX, 42MX, and 54SX devices the register setup is included in the reported delay (shown in the Paths tab, as in Figure 2-1 on page 22). These devices use the input-to-input timing model, as explained on page 5.

For the devices that use the pin-to-pin timing model, including 54SX-A, eX, Axcelerator, and Flash devices, the delay is reported until the input pins of the registers. Therefore, the setup time is not included in this delay. However, the register setup and hold, as well as the clock skew, are taken into account during the analysis of setup check and hold check when identifying timing violations. Setup, hold, and clock skew are also taken into account during clock frequency estimation.

For information on the setup and hold process in Timer, see the Expanded Paths window ("Expanding Paths" on page 28). It enables you to view clock network insertion delay and clock skew information.

For more information on displaying detailed path analysis and expanded paths, please refer to "Detailed Path Analysis" on page 21.

PLLs

The timing tool sees a PLL as a register and a clock generator. Any clock output port in a PLL is a potential clock (and appears in the list of potential clocks for the design). Like all other potential clocks, you can constrain these PLL output clocks by setting any clock constraint independently. The input clock of the PLL on which you set the constraint is not the clock input port of the PLL. Instead, it is the clock that drives the clock input port. The driving clock is always a Primary port of the design, a register's output, or another PLL's output.

Axcelerator Device Family Only: By default, when you set a clock constraint on the clock source connected to the clock input of the PLL, Timer automatically computes the clock constraints on the outputs of the PLL (according to the PLLs configuration). Thus, the value of the clock output is equivalent to the clock input multiplied, divided, or shifted by the value of your static configuration.

Note: For ProASIC devices, the PLL is only considered as a register; there is no output clock computation.

If you specify a clock constraint for the output clock(s), the PLL ignores the static configuration value and delivers a clock frequency according to your constraints. Timer reports this value accurately. In addition, if you remove your constraints on the output clock(s), the Timer tool recalculates your output frequency according to your static configuration value. For more information on generating PLLs and their logic characteristics, please refer to the *Guide to ACTgen Macros*.

RAMs, and FIFOs

The Timer tool displays blocks of RAM and FIFO as a single "black box," (you have as many black boxes as you have instantiations of RAMs and FIFOs in your design). Thus, if you construct a RAM or FIFO cell out of several RAM blocks, Timer sees and treats the cell as a single black box. Timer does not display timing information within individual black boxes, because all the delays

are reported using the interface of the RAM. Timer displays timing information between black boxes and other logic in the design.

Timer treats RAMs and FIFOs as registers, and like any register, they have clock signals. For more information about RAMs and FIFOs, please refer to the *Guide to ACTgen Macros.*

RAM

The Axcelerator family supports dual-port RAM; you can write and read RAM at the same time, but not to the same address.

FIFO

Timer displays the paths to the FIFO flags depending on their clock. Timer shows paths to Empty and Almost Empty with respect to the Read clock; paths to Full and Almost Full are displayed with respect to the Write clock.

2

Using Timer

This chapter contains information on how to use Timer to analyze timing performance and set timing constraints. For an introduction to Timer's interface, please refer to "Getting Started with Timer" on page 9.

Determining Your Clock Frequency

Because a design's performance is often measured through the clock frequency, determining the clock frequency is the most common use of static timing analysis.

To obtain the frequency of a specific clock:

1. **Click the Summary tab in the Timer window.**
2. **Select a clock from the Clock pull-down menu.** The selected clock becomes your current clock. The frequency is displayed under the speedometer.

   The clocks listed in the pull-down menu are defined as signals which drive the clock or gated input of two or more adjacent registers. For families that use the pin-to-pin timing model, one register is enough to have the clock listed as a potential cock. Virtual clocks are not supported.

   In frequency calculations, values for latency is assumed to be 0, the duty cycle is 50%, and the clock edge is rising. (You can set the duty cycle in the Clocks tab.) For pin-to-pin timing model families, Timer takes into account the register setup and the clock skew (starting in R1-2003) when estimating the maximum clock frequency. However, the setup value is not included in the actual delay reported between the clock pin of a source register and the data pin of a sink register. For more information on calculating delays, please refer to "Calculating Delays with Timer" on page 17.

Detailed Path Analysis

Timer organizes and displays data based on your timing analysis preferences (see "Setting Preferences" on page 35). Timer assists you in analyzing critical paths, paths with the greatest delay, and by expanding paths so you can trace delays along paths.

Displaying Paths

Path sets (groups) and paths within each set are displayed on the Paths tab. You can create your own sets and add them to the paths tab (see "Adding Path Sets" on page 23). Also, Timer displays all previously entered sets that have a constraint in the Set grid.

To display paths:

1. **Click the *Paths* Tab.** By default, Timer displays four path sets in the set grid.
2. **Click a set.** Timer displays the paths in the path grid.

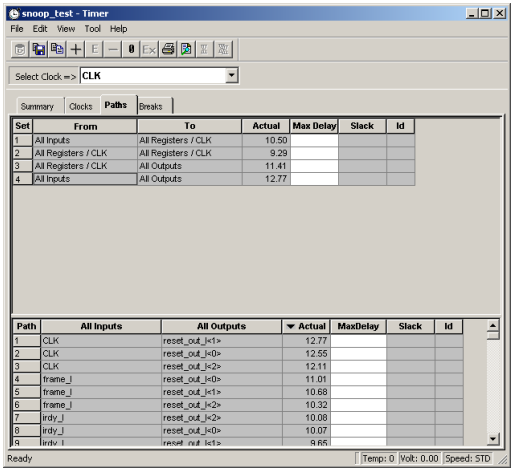

Figure 2-1. Timer Paths Screen

Note: When you set a clock constraint for a pin-to-pin timing model family, it is mapped into specific register to register max delay values; these values appear in the max delay of each specific path in the spreadsheet. Timer takes into account register setup and clock skew when computing max delay values for these pin-to-pin model families.

The register-to-register selections are based on the clock domain selected in the Clocks tab. (To select another clock, click the Clocks tab and select another clock from the drop-down Clock Name menu.)

All delays shown are worst-case by default. To change this setting, see "Displaying Best, Worst, or Typical Case Analysis" on page 39.

The Paths tab displays the following timing information:

- **Actual:** The actual delay calculated by Timer for each path.
- **Max Delay:** The maximum required delay entered. Max Delay always displays the tightest constraint specified, regardless of how many constraints you have entered. Note that clock constraints may be translated into Max Delay values and appear in this column.
- **Slack:** The difference between the maximum required delay and the actual delay.
- **ID:** The constraint ID automatically assigned to the path.

Adding Path Sets

Create and add path sets to the Paths tab to determine delay information and enter constraints. User-defined sets enable you to customize the sets that are available for analysis. By creating custom sets, you can simplify timing analysis and constraint setting for specific blocks or paths in your design.

For example, if you are concerned about timing of the lower-level block "sub_block_1" in your design, you can create a set that only includes timing paths in that block.

To add a set:

1. **Click the Paths tab.**

2. **From the Edit menu, click *Add Set of Paths*.**

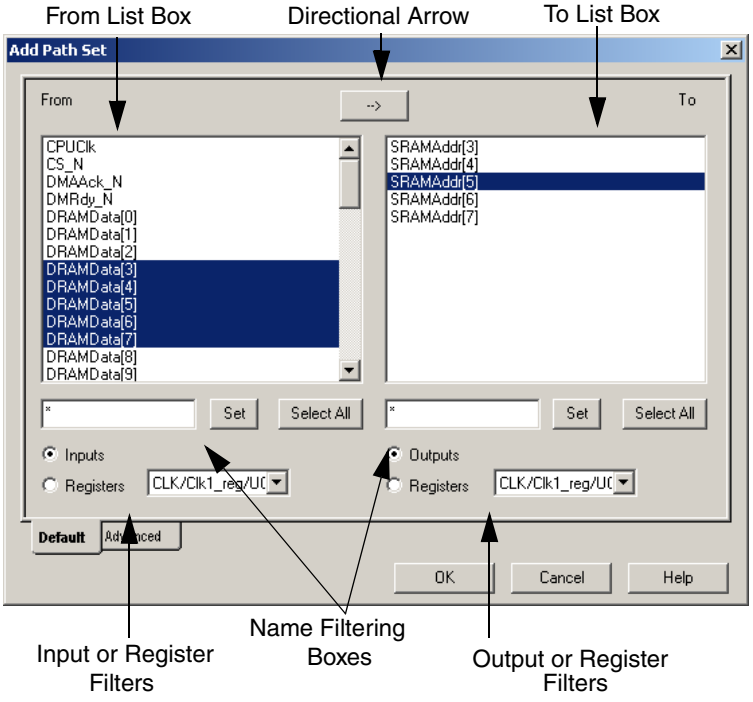

Figure 2-2. Timer Add Set Dialog Box

The Add Path Set dialog box consists of two screens, Default and Advanced. The Advanced screen enables you to use keywords to create a set (see for "Using Keywords to Create and Add Sets" on page 26).

3. **Select the desired clock.**
4. **Click the directional button to select path direction.**
5. **Select the desired Inputs, Registers, and Outputs radio buttons to filter the From and To list boxes.** The example in Figure 2-2 on page 24 shows Inputs in the From list box and All Registers in the To list box.

   - **Inputs:** All of the input pad pins.

- **Outputs:** All of the output pad pins.
- **Registers:** All input pins on the flip-flops and latches. Use the pull-down menus to choose the active clock nets. Choose "All" for both to find delays for all register-to-register paths.

6. **Select your desired starting and ending points in the From and To list boxes.** Naming filters are provided to limit the list of terminals for consideration. The naming filters use the * character as a wildcard and the / character to delimit levels of hierarchy. For example, use * to filter for all terminals; *:E to filter for all terminals with pin E; U1/* to filter for all terminals in block U1; and U1/*:E to filter for all terminals in block U1 with a pin E. You can also use multiple wildcards such as */U1/*:E. After entering your naming filter, click the Set or Select All button.

   If the directional button is pointing right, then:

   - Select a starting point in the From list. The To List Box displays all corresponding endpoints.
   - Select one or more endpoints in the To list box that complete the path set. Click the Select All button to select all endpoints.

   If the directional button is pointing left, then:

   - Select the endpoint in the To list box. The From list box displays all corresponding starting points.
   - Select one or more starting points in the From list box. Click the Select All button to select all.

7. **Click *Apply* to add the path set to the Paths tab.** Continue creating and adding sets. When you are done, click OK to close the Add a Set dialog box.

Adding a Set That Shows One Input to All Outputs

To show one input to all outputs, you must add the set to the Paths tab. You can then view delay details and set constraints.

To show one input to all outputs:

1. **Click the Paths tab.**
2. **Choose *Add Set of paths* from the Edit menu.** The Add Path Set dialog box appears, as shown in Figure 2-2 on page 24.

3. **Select the Inputs and Outputs radio buttons.**
4. **Click to directional arrow to point it right, from Inputs to Outputs.** Click the directional arrow to change direction.
5. **Choose the desired input starting point in the From list box.**
6. **Select all outputs by Clicking on the Select All button under the To list box.**
7. **Click OK.** The set showing one input to all outputs is added to the Paths tab.

Adding A Set Showing All Inputs to One Output

To show all inputs to one output you must configure and add the set to the Paths tab.

To create a set showing all inputs to one output:

1. **Click the *Paths* tab.**
2. **From the Edit menu, click *Add set of paths*.** The Add Path Set dialog box will appear, as shown in Figure 2-2 on page 24.
3. **Select the Inputs and Outputs radio buttons.**
4. **Click the directional arrow to point it left.**
5. **Choose the desired output endpoint in the To list box.**
6. **Select all inputs, all starting points, by Clicking on the Select All button under the From list box.**
7. **Click Ok.** The set showing all inputs to one output is added to the Paths tab.

Using Keywords to Create and Add Sets

The Advanced tab in the Add Set dialog box enables you to use keywords (macros that represent various sets of terminals) to create a set.

Note: Supported keywords and their usage for the SX-A, eX, and ProASIC families is explained in Appendix A on page 49.

Supported keywords include:

- $inputs()

  All input and bi-directional pins.

- $outputs()

  All output and bi-directional pins.

- $registers(clock_name)

  The pins of all registers driven by the clock whose name is clock_name.

To create a set using keywords:

1. **Click the *Paths* tab.**
2. **In the Edit menu, click Add Set of Paths.**
3. **Click the *Advanced* tab (Figure 2-3).**

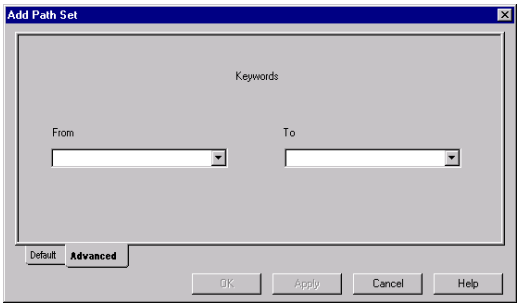

Figure 2-3. Add Set Dialog Box

4. **Enter the From keyword or choose a keyword from the From drop-down list box to define the From set.**
5. **Enter the To keyword or choose a keyword from the drop-down list box to define to To set.**
6. **Click OK.** This displays paths for the keyword set in the paths tab.

To edit a path set:

1. **Select the Set in the Paths tab.**

2. **In the Edit menu, click *Edit Set of Paths*, or right click and choose *Edit Set*.** The Edit Set dialog box is displayed.
3. **Edit the *Path* set and click *OK*.**

To remove a path set:

1. **Select the set in the Paths tab.**
2. **In the Edit menu, click *Remove Set of Paths*, or right-click and choose *Remove Set* from the right-click menu.** The set is removed.

Expanding Paths

Each path has one or more logic macros that contribute to its total delay. By expanding the path, you can view detailed delay information for parallel paths.

Note: With the exception of parallel edges, parallel paths are not available for families that use the pin-to-pin timing model (see page 5 for an explanation of pin-to-pin and input-to-input timing models).

To expand a path:

1. **Click the *Paths* tab.**
2. **Select a Path set in the path set grid.** Paths within that set are displayed below in the path grid.
3. **Select the path you wish to expand.**
4. **Expand the path by double-clicking the path, right-click and select "Expand Path" from the shortcut menu, or in the Edit menu, click *Expand Path*.** The Expanded Paths window (Figure 2-4)

opens and displays a single path in the Expanded Paths window, as shown in Figure 2-4.

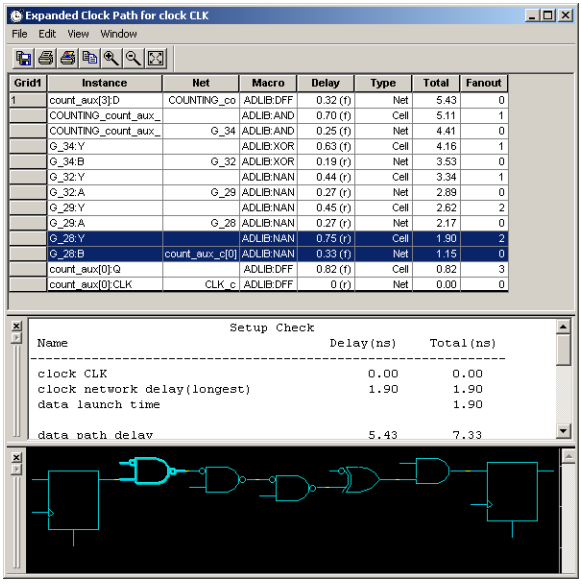

Figure 2-4. Timer Expanded Paths Window

The Expanded Paths window is comprised of three components:

- Expanded Paths Grid - Shows all delay components for the selected path (Instance, Net, Macro, Delay, Type, Total Delay and Fanout details). For Delay, (r) stands for rising edge and (f) for falling edge. If you expand a register to register path, the Expanded Path window displays relevant register setup timing information.
- Setup Check / Hold Check window - Set the Show option (in Preferences) to “Longest” to view a detailed analysis of the Setup Check, as in Figure 2-4. Set the Show option to “Shortest” to view a detailed analysis of the Hold Check. (These analyses include clock insertion delay information.)
- Expanded Paths Schematic - Displays a schematic view of the expanded path.

In addition, the Expanded Paths window contains toolbar buttons (Figure 2-5) that enable you to:

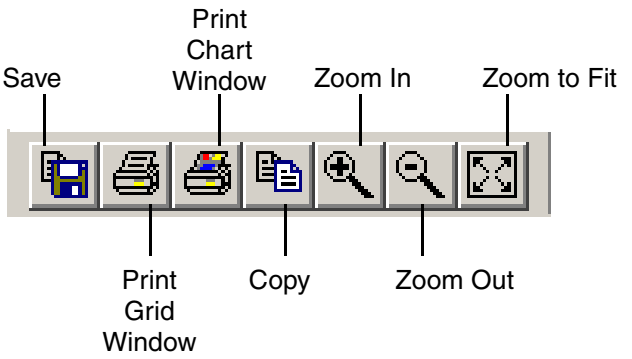

Figure 2-5. Expanded Path Window Toolbar Buttons

Save: Save the contents of the Grid as a .txt file

Print Grid Window: Print the contents of the Grid window

Print Chart Window: Print the contents of the Chart window

Copy (Grid to Clipboard): Copy the contents of the Grid window to the clipboard

Zoom In: Click to zoom on the Chart window

Zoom Out: Click to zoom out on the Chart window

Zoom to Fit: Click the Zoom to Fit button to automatically fit the entire path in the Chart window

Note: The expanded paths window for eX, SX-A, Axcelerator, and ProASIC devices shows the expanded path on a pin-to-pin basis rather than an input-to-input basis. There is a separation between the module delay and the net delay.

Anything you select in the Expanded Paths grid or Graph window is reflected in both windows.

- Selecting the path number in the Expanded Paths grid highlights the entire path in the Chart window.
- Selecting an instance, net, or macro in the Expanded Paths grid

highlights that selection in the Chart window.

- Selecting a logic macro in the Chart window, highlights all instances of the macro in the Expanded Paths grid.

Toggle the Graph Window on and off by choosing Graph Window from the Window menu. Use the View command menu to Zoom in and out. In the Graph window, dragging the mouse downward and to the left will zoom fit. Dragging downward and to the right drags out a zoom in area.

In some cases, long instance names may overlap and be difficult to read in the Graph window. This problem can be solved by moving the module. To move the module, select the module and while holding down the Shift key, click and drag the module to another location.

Using ChipEdit with Timer

Use ChipEdit and Timer together to view placement-and-routing of Timer paths in ChipEdit.

Note: This feature is not available for ProASIC devices.

To view critical paths:

1. **Open Timer and ChipEdit from Designer.**
2. **In Timer, click the Paths tab.**
3. **Select a Path set in the path set grid.** Paths within that set are displayed below in the path grid.
4. **Select the path you wish to expand.**
5. **Expand the path.** To do so, double-click the path, click the Expand button. The Expanded Paths window (Figure 2-4) opens and displays a

single path in the Expanded Paths Grid and a graphical representation of the paths in the Chart Window, as shown in Figure 2-6**.**

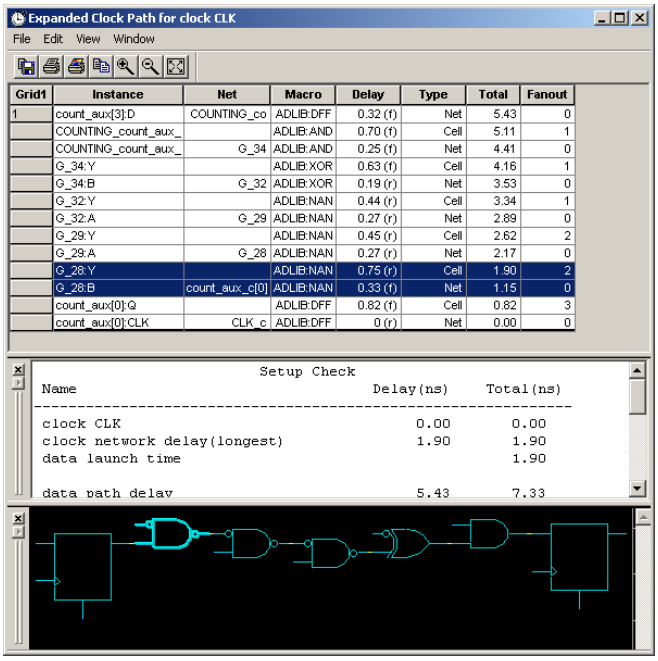

Figure 2-6. Timer Expanded Paths Window

The Expanded Paths grid shows all delay components for the selected path (Instance, Net, Macro, Delay, Type, Total Delay and Fanout details). For Delay, (r) stands for rising edge and (f) for falling edge.

Anything you select in the Expanded Paths grid or Graph window is reflected in both.

- Selecting the path number in the Expanded Paths grid highlights the entire path in the Chart window.
- Selecting an instance, net, or macro in the Expanded Paths grid highlights that selection in the Chart window.

- Selecting a logic macro in the Chart window, highlights all instances of the macro in the Expanded Paths grid.

Toggle the Graph Window on and off by clicking *Graph Window* from the Window menu. Use the View command menu to Zoom in and out. In the Graph window, dragging the mouse downward and to the left will zoom fit. Dragging downward and to the right drags out a zoom in area.

Note: In some cases, long instance names may overlap and be difficult to read in the Graph window. This problem can be solved by moving the module. To move the module, select the module and while holding down the Shift key, click and drag the module to another location.

6. **Select a module or net in the Expanded Paths dialog box.** The module or net is shown in ChipEdit, as shown in Figure 2-7**.**

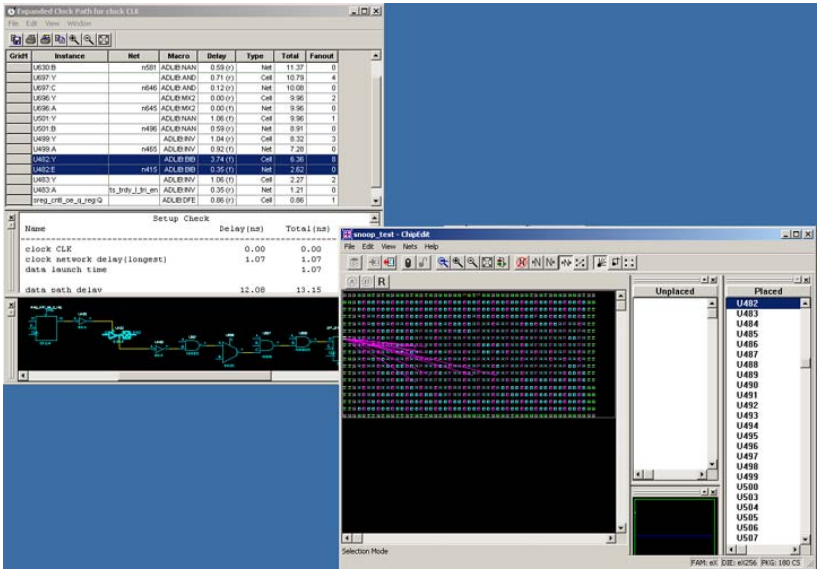

Figure 2-7. Timer and ChipEdit

Adding and Removing Break Points

Without stop points, you see all the paths from pad to pad in the design. If you do not want to see the paths going through registers clock pins, you could specify these as stop points. The path going through those pins would not be displayed.

Setting a pass on a module pin will enable you to see a path through individual pins. Additionally, you can set global pass on all Clk/G and Clr/Pre pins in the Preferences dialog box, which is available by choosing Preferences from the File menu.

To add break points:

1. **Click the *Breaks* tab.**
2. **Select Global Stops or Pass Pins.** The All Pins list box displays the pins, as shown in Figure 2-8.

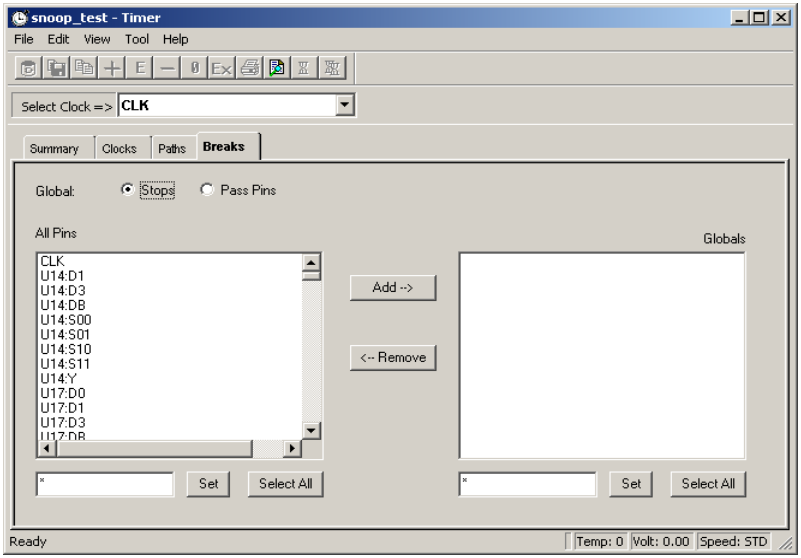

Figure 2-8. Breaks Tab, Stops Selected

3. **Select Pin(s). The All Pins list box defaults to show all pins.** Text boxes are provided below the list boxes to help you limit the list for consideration. Enter a value and click *Set*. The * character is used as a

wildcard. To select multiple pins, hold down the CTRL key while selecting with your mouse. Click *Select All* to select all pins displayed in the All Pins list box.

4. **Click *Add*.** The Stops or Pass Pins will be added to the Global list box as break points.

To remove break points:

1. **Click the *Breaks* tab.**
2. **Select Global Stops or Pass Pins**. The break points are displayed in the Global list box.
3. **Select break Points to remove.** To select multiple breaks, hold down the CTRL key while selecting with your mouse. Click Select All to select everything displayed in the Global list box.
4. **Click *Remove*.** The pin(s) will be removed and appear in the All Pins list box.

Setting Preferences

Use the Preferences dialog box to set your display and timing analysis preferences. For UNIX users, the summary of commands is as follows:

```
report -type timer
[-sortby {actual,slack}]
[-maxpaths <num>]
[-case {worst,typical,best}]
[-path_selection {critical,any_pair}]
[-setup_hold {on,off}]
[-expand_failed {on,off}]
[-clkpinbreak {on,off}]
[-clrpinbreak {on,off}]
[-latchdatapinbreak {on,off}]
[-slack <num>]
```

Calculating Delays

You may wish to prevent Timer from calculating delays during initialization. (By default, Timer estimates all potential clock frequencies, as well as the 4 delays corresponding to the 4 primary sets

(All inputs to All outputs, All inputs to registers, registers to All outputs, registers to registers) associated with the slowest clock during initialization.)

To change your option for pre-calculating delays, from the File menu, select Preferences (Figure 2-11), and deselect "Precalculate delays." Alternatively, you may choose to modify the related variables. To do so, from the Designer GUI, in the Options menu, select "Set Variable." In the Variable Name dialog box, enter:

```
TIMER_PRECALCULATE_DELAYS
```

And in the Value dialog box, enter

```
0
```

(default is "1").

Changing the Number of Paths

Use the Preferences dialog box to control the number of paths displayed in the Paths tab and Expanded Paths windows.

To change the number of paths displayed:

1. **In the File menu, click *Preferences*.** The Preferences Dialog Box appears, as shown in Figure 2-9**.**

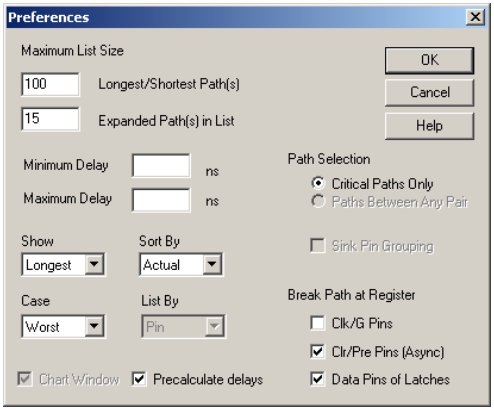

Figure 2-9. Timer Preferences Dialog Box

2. **In the Maximum List Size area, enter your default preferences for the maximum number of Longest/Shortest Path(s) and Expanded Path(s) that you want to display.** The maximum value for Longest/Shortest Path(s) is 200.
3. **Click *OK*.**

Displaying the Shortest Paths First

By default, Timer displays the first 100 paths from longest to shortest. When longest is selected, setup times will be reported for registers. When shortest is selected, hold times will be reported.

To display the shortest paths first:

1. **In the File menu, click *Preferences*.** The Preferences Dialog Box appears, as shown in Figure 2-9 on page 36.
2. **Select Shortest from the Show drop-down menu.**
3. **Click *OK*.**

Setting Minimum or Maximum Delay Filters

Use the Preferences dialog box to filter paths for delays above, below, or between a specified value. Enter your display preferences in the Maximum Delay and Minimum Delay boxes and click *OK*.

Sorting and Displaying by Actual or Slack Delays

Timer can display delay information in two ways:

- Actual delay values
- Slack, which is the difference between actual delay and a user-specified delay (that is, user-specified constraint)

Displaying by Actual Delay

The actual delay is the path delay between two points in your design. This is the only way to sort your data if you do not have any timing constraints entered (for information on setting timing constraints, see "Timing Constraints" on page 40). If you have entered timing constraints, the actual

delay report will automatically display the slack - even if you don't ask for it - but the data will always be listed from longest to shortest actual delay.

Actual delay measurements may be calculated before or after layout (delay measurements calculated only after layout for ProASIC devices).

To display actual delay,

1. **In the File menu, click *Preferences*.** This displays the Preferences dialog box is (see Figure 2-9 on page 36).
2. **Select Actual in the Sort By pull-down menu.**
3. **Click *OK*.**

Displaying by Slack Delay

Slack delay is the delay difference between a timing constraint entered in Timer and the actual delay of a path. For example, if a signal takes 20 ns to get from point A to point B, and you entered a timing constraint of 15 ns, the Timing Report would list -5 ns slack for that path. Thus, if the slack negative, then the actual delay did not meet the desired timing by the absolute value of the slack (in ns). Conversely, if the slack value is positive, then the timing constraint was met, with the slack value (in ns) to spare. In a slack report, Timer sorts the data (by default) from longest to shortest slack.

When displaying slack, all the paths without timing constraints are filtered from the reported data. This enables you to quickly determine how well your design meets your timing requirements. This is especially useful for viewing critical delays like register-to-register, clock-to-out, and input-to-register.

To display slack delay:

1. **In the File menu, click *Preferences*.**
2. **Select Slack in the Sort By pull-down menu.**
3. **Click *OK*.**

Displaying Best, Worst, or Typical Case Analysis

By default, Timer displays the worst case analysis.

To display the best or typical case analysis:

1. **In the File menu, click *Preferences*.** The Preferences Dialog Box appears, as shown in Figure 2-9 on page 36.
2. **Select Best, Typical, or Worst from the Case drop-down menu.** If you change the setting, Timing is recalculated for the entire design; this may take a few minutes.
3. **Click *OK*.**

Path Selection

Normally, Timer displays only critical paths. Critical paths are the longest path between any of the starting points (terminals) and each ending terminal. If you would like to see the timing of all paths between any of the starting terminals and any of the ending terminals, select Paths Between Any Pair in the Path Selection area of the Preferences dialog box, Figure 2-9 on page 36. Selecting Critical Paths causes only the critical paths to be displayed.

Adding and Removing Break Paths

By default Timer displays paths that break at all clock, gate, clear, and preset pins. If you would like to display paths that pass through these pins, un-select the appropriate pins in the Break Path at Register options in the Preferences dialog box, as shown in Figure 2-9 on page 36.

Excluding Certain Paths

Asynchronous feedback paths in a design can cause paths to be reported as having excessive delays. The most common example is feedback paths through asynchronous Set or Reset Pins to banks of flip-flops, like a state machine or a counter.

To exclude certain paths:

1. **In the File menu, click *Preferences*.** The Preferences Dialog Box appears, as shown in Figure 2-9 on page 36.

2. **Break Paths at Register.** Choose Clk/G Pins, Clr/Pre Pins (Async) or Data Pins of Latches to prevent displaying paths that pass through either clock, gated, clear, preset, or data pins of flip-flops or latches.
3. **Click *OK*.**

Timing Constraints

Timer enables you to specify timing constraints and requirements for clocks and paths. Use these constraints to generate timing reports, back annotate timing information, and for use in Timing Driven Layout. In order to run Timing Driven Layout, you must enter and commit your constraints in Timer before exiting timer.

Delay Constraint Guidelines

Delay constraints control the Timing Driven Layout engine. You can define these constraints using Timer or by importing an external DCF or SDC file. The Timing Driven Layout engine considers the defined delays when allocating silicon resources with the goal of meeting or beating all constraints if possible. The Timing Driven Layout engine evaluates the performance criticality of one function versus another when allocating device resources. Because resources are limited, use the following guidelines to ensure the defined constraints meet the needs of the design without impairing device resources.

Set Sufficient Constraints

All constraints for the design should be defined to ensure correct operation of the Timing Driven Layout engine. Timing Driven Layout considers networks that have not been defined as “don't care” paths, which have a low priority for resource allocation. If these undefined paths are actually critical, they may fail to meet performance demands. Adding constraints incrementally may cause performance problems in other undefined networks.

Avoid Unnecessary Constraints

Describe “don’t care” paths to free high performance device resources. Not defining a path is one mechanism for doing this. However, it is difficult to avoid defining some “don't care” paths, so Designer

provides clock exceptions and global stop sets to enhance this capability (see "Clock Exceptions" on page 42).

Avoid Overconstraining

The Timing Driven Layout engine is designed to achieve or exceed the delay constraint defined (less than or equal). Defining a constraint shorter than is actually required for margin can have a negative impact on the performance of the device because of competition for device resources.

Delay Constraint Definitions

A description of delay constraint methodology requires the following terms:

- **DTL terminals:** Timing Driven Layout terminals define the starting (or source) and ending (or sink) points for a signal path. They are always I/Os or sequential elements; no intermediate combinatorial element is currently supported as a terminal.
- **Signal Path:** The signal path describes a consecutive sequence of logic and nets, the first net being driven by a start terminal, and the last net driving a macro input pin of the end terminal.
- **Network:** A network can consist of 1 or more start terminals and 1 or more end terminals. All signal paths connecting any start terminal to any end terminal are included in the network. Only one delay value can be assigned to each defined network. Networks can be defined implicitly by a common clock (synchronous network) or explicitly by a defined set of terminals. Network and Paths are used interchangeably.
- **Path Delay:** The path delay defines the sum of all the individual delays of the nets and the logic macros in the signal path.
- **Delay Constraint:** A delay constraint defines a fixed amount of time required for a signal to propagate from all starting terminals to all ending terminals for a network.
- **Don't Care Path:** A signal path in which the delay is considered to be infinite.
- **Global Stop:** A defined intermediate point in a network that forces all paths through the defined point to be don't care paths regardless

of any constraint assignment.

- **Clock Exception:** A terminal in a synchronous network that should be excluded from the specified clock period. The exception can remain undefined (don't care) or can be assigned a unique value in the Path Constraint Editor.

Specifying Clock Constraints

Use the Clocks tab to assign values to each clock network in your design.

To assign clock constraints:

1. **Click the *Clocks* tab.**
2. **Select the clock of interest in the Clock Name pull down menu in the toolbar.**
3. **Specify the timing requirements.** In the Constraints area, define the Required and Duty Cycle areas**.** Select MHz or ns from the pull-down menu.
4. **Click *Set*.**

Clock Exceptions

Timer enables you to specify global clock constraints. If you have paths that are not required to meet the global constraint (for example, multi-cycle paths), then you should list them as exceptions. The Clocks Exceptions area on the Clocks tab provides a mechanism for doing this. A terminal specified as a clock exception will cause all paths beginning or ending at this terminal to be unconstrained by the global timing constraint.

To add or remove terminals from the Clock Exception List:

1. **Click the *Clocks* tab.**
2. **Select the Clock name from the drop down menu.**
3. **Enter a constraint in the Constraints area and click *Set*.**
4. **Select Source or Sink in the Clock Exceptions area.** The Clock Exceptions area displays the Pins. The terminals of the sequential device are

displayed using an <instance_name>:<pin_name> format. For example, a DFM with an instance name of U1\FF1 will have a single source terminal, U1\FF1:CLK, and 3 three sink terminals: U1\FF1:A, U1\FF1:B, and U1\FF1:S.

5. **Use the Filter Field to further sort the list of clock pins.** Naming filters are provided to limit the list of terminals for consideration. The naming filters use the * character as a wildcard and the / character to delimit levels of hierarchy. For example, use * to filter for all terminals; *:E to filter for all terminals with pin E; U1/* to filter for all terminals in block U1; and U1/*:E to filter for al terminal in block U1 with a pin E. After entering your naming filter, click the *Set* or *Select All* button. Multiple * and / characters may be used.
6. **Add or Remove the clock exception.** To add a clock exception, highlight the desired entry from the Clock Pins list and click *Add*. To remove an exception, highlight it in the Exceptions list and click *Remove*.
7. **From the File menu, select Commit to commit changes.**

Specifying Path Constraints

You can specify a timing constraints on a specific path or groups (sets) of paths.

To specify a timing constraint for a path set:

1. **Click the *Summary* or *Paths* tab.**
2. **Select a Path set.**
3. **Enter the timing constraint.** On the Summary tab enter the constraint in the Required text boxes and click *Set*. On the Paths tab enter the constraint in the Max Delay column.

To specify a timing constraint for a specific path:

1. **Click the *Paths* tab.**
2. **Click the corresponding set in the Set grid.**
3. **Select the path in the path grid.**
4. **Enter the timing constraint in the Max Delay column.**

Removing Constraints

You can remove all constraints or just selected constraints. To remove all constraints choose Remove All Constraints from the Edit menu.

To remove select constraints on the Paths tab:

1. **Click the *Paths* tab.**
2. **Select the path set with the constraint you wish to remove.**
3. **In the Edit menu, click *Remove Selected Constraints*.**

To remove select constraints on the Summary tab, delete the constraint in the Required control box and click *Set*.

Timing Results

Exporting Results

From the Paths tab, you can export the path or set grids in a text file.

To save your results to a text file:

1. **Click the *Paths* tab.**
2. **In the File menu, click *Export Path Grid* or *Export Set Grid*.** The Save As dialog box is displayed.
3. **Choose a destination on your disk, enter a File Name and click *Save*.**

Committing and Exiting

If you wish to save the constraint requirements entered into Timer, you must commit your Timing results before exiting Timer.

To commit your results choose Commit from the File menu before exiting, or click *Yes* when asked if you would like to commit your results before exiting. Timer saves your timing constraints to Designer's temporary design database.

Generating Timing Reports

The timing report enables you to quickly determine if any timing problems exist in your design. The timing report lists the following information:

- Delay from input I/O to output I/O (longest or shortest, depending on your Preferences).
- Delay from input I/O to internal registers (longest or shortest, depending on your Preferences).
- Delay from internal registers to output I/O (longest or shortest).
- Delays for each clock network (longest or shortest).
- Delays for interaction between clocks networks (longest or shortest).

To generate a timing report:

1. **In the Tools menu, click *Report Paths*.** The Timing Report dialog appears. You have the following options:

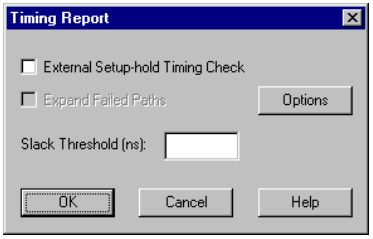

Figure 2-10. Timing Report Dialog Box

   - To include external setup and hold timing, select the External Setup hold Timing checkbox. Selecting the External Setup hold timing checkbox adds specific sections to the timing report, including External setup and hold as well as clock-to-out timing information.
   - If you select Sort By Slack in the Preferences dialog box, you can also limit the number of delays displayed based upon the Slack threshold. For example, if you want to see only the delays which have a slack less than 5 ns, select Slack in the Sort by drop-down list box in the Preferences dialog box and then enter 5 in the Slack Threshold text box in the Timing Report dialog box. The timing report will display all the timing paths that have a slack of 5 ns or less (that is, all paths that met the timing constraints

by at least 5 ns as well as all the paths that failed to meet constraints). If you would like to display the timing paths that failed by 10 ns or more, enter -10 in the Slack Threshold box; the timing report will display the paths that failed to meet the timing constraints by 10 ns or more.

2. **For additional Timing Report Options, click the *Options* button.** This displays the Preferences dialog box, as shown in Figure 2-11.

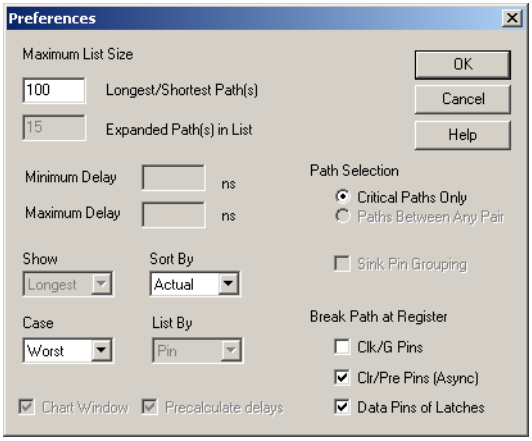

Figure 2-11. Preferences Dialog Box

3. **Select analysis preferences.** The default settings are shown in Figure 2-11. You have the following options for your Timing Report:

   - If you are interested in exploring conditions other than Worst case, use the Case drop-down menu to select either Typical or Best.
   - To change the number of timing paths displayed in the report, enter the desired number in the Maximum Paths box (default is 100) and the Expanded Path(s) box (default is 15).
   - If you have entered timing constraints ("Timing Constraints" on page 40), you may use the Sort By option to sort the delays according to either actual or slack delays.(See "Sorting and Displaying by Actual or Slack Delays" on page 37).
   - Normally, only the longest path between any of the starting

points (terminals) and each ending terminal is displayed. If you would like to see the timing of all paths between any of the starting terminals and any of the ending terminals, select Paths Between Any Pair in the Path Selection box.

- The default timing paths break at all clock, gate, clear, and preset pins. If you would like to generate a timing report that passes through these pins, un-select the appropriate pins in the Break Path at Register options.

4. **Once you are satisfied with your selections, click *OK* in the Preferences dialog box and then click *OK* in the Timing Report dialog box.** The timing report is displayed in a separate window.

Generating Violations Reports

For families that use the pin-to-pin timing model, the Violations report enables you to obtain constraint results sorted by slack. You can now view Max Delay violations as well as Min Delay violations in the report.

A

Using Keyword Filters

This appendix is a reference guide for the use of keywords in Timer. The use of keywords is only supported for pin-to-pin delay families (for a an explanation of pin-to-pin and input-to-input delay families, see page 5). Use keywords to create custom sets for Timer's Paths tab screen. Refer to "Using Keywords to Create and Add Sets" on page 26 for details on how to enter keywords.

Keywords enable you to filter out any unwanted paths or instances, making it easier to view critical paths in the design and limiting the paths displayed for a particular set. Timer uses two types of keywords, first- and second-level.

Levels of Keywords

The first-level keywords enable access to the main objects of the design, such as registers, while the second-level keywords enable access to a sub-list of these main objects. For instance, *$registers()* is a first-level keyword that enables access to all the registers of the design. This list includes clock pins, data pins, enable pins and, asynchronous pins.

If the *$registers()* keyword is combined with the second-level keyword *$datapins()*, the related command is applied only to the data pins of the registers. You can use a second-level keyword only with a first-level; second-level keywords may not be used alone. In Timer, only the first-level keyword *$registers()* may be combined with the second-level keywords. Use the colon ":" without any spaces to combine first- and second level keywords. Keywords and filters are case insensitive.

Filtering

Filter keywords with brackets [ ]. The filter is a string that is used as an identifier (it may contain wild cards). [ ] with an empty string is not accepted in the macro language. The user can enter $registers(), $registers()[*filterString*], but not $registers()[ ].

Functions

Sometimes you may want to locate objects of the design by defining or identifying other objects. For instance, you might want to analyze delays of all the registers driven by a specific primary clock. Functions can help you locate the registers (objects) by defining the primary clock (identifier).

To use functions, the identifier of the object has to be reported between parentheses ( ). This identifier may contain wild cards and can also be another keyword. For example:

$registers(clock1)	returns all the registers driven by the primary clock "clock1"

Supported Keywords

Timer supports the keywords listed in Table A-1.

Table A-1. First- and Second-Level Keyword Summary

First-Level Keywords	Second-Level Keywords
$registers()	**$datapins()**
$inputs()	**$clockpins()**
$outputs()	**$asyncpins()**
$clocks()	**$enablepins()**
$ports	**$outputpins()**
	$inputpins
	$allpins

First-Level Keywords

Each keyword has two identifiers, a long version and a short version. They both have exactly the same function. The first-level keywords are defined below.

`$registers(ClockName)` or `$reg(ClockName)`

The keywords above only display the registers (edge-triggered flip-flops and level-sensitive latches) controlled by the clock *ClockName*. If no *ClockName* is specified, this keyword will cause all the registers of the design to be displayed.

`$inputs()` or `$in()`

This keyword only displays all the primary inputs of the design.

`$outputs()` or `$out()`

This keyword only displays the primary inputs of the design.

"$Clocks()" or "$CK()" only displays the primary clocks of the design.

`$ports(`*`InstanceName`*`)` or `$po(`*`InstanceName`*`)`

This macro replaces all the primary inputs and outputs of the design.

Second-Level Keywords

While first-level keywords allow access to the main objects of the design, such as registers, second-level keywords give access to a sub-list of these main objects.

Currently, second-level keywords can only be used with the first-level keyword *$registers()*. A first-level keyword is separated from a second-level keyword with the colon ":" character, without any white space.

As with first-level keywords, each second-level keyword has two identifiers, a long version and a short version. Each has the exact same function. In the following examples, it is assumed that the notion of event and pin are implicit.

"$DataPins()" or "$dp ()" indicates all the data pins of a register. For example:.

`$registers(CLK):$dp()`	displays the data pins of all the registers controlled by CLK

"$OutputPins()" or "$qp()" indicates all the output pins of a register. For example:.

$registers(CLK):$qp()	displays the output pins of all the registers controlled by the primary clock CLK

"$ClockPins()" or "$cp()" indicates all the clock pins of a register. For example:.

$registers(CLK):clockpins()	displays the output pins of all the registers controlled by the primary clock CLK.

"$AsyncPins()" or "$ap()" indicates all the asynchronous pins of a register (preset and clear).

"$EnablePins()" or "$ep()" indicates all the enable pins of a register. For example:

$registers(CLK):$ep()	displays the enable pins of all the registers controlled by the primary clock CLK.

$inputpins() or $ip() indicates all the input pins of a register. For example:.

$reg(CLK):$inputpins()	Displays the input pins of all the registers controlled by the CLK

$allpins() indicates all the input pins of a register. For example:.

$registers(CLK):$all-pins()	Displays the pins of all the registers controlled by the CLK

Second-Level Exceptions

In order to provide more flexibility, the second level keywords can be coupled with exceptions. For instance, if the you want to select all the input pins of the registers except the clock pins, you can use the following macro:

$registers(clk):$inputpins(TmacEx_CLOCKPINS)

The available exceptions are listed in the following table:

Table A-2. Second-Level Exceptions

Exception	Result
TmacEX_CLOCKPINS	The clock pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_DATAPINS	The data pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_SYNCPINS	The synchronous pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_ASYNCPINS	The asynchronous pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_INPUTPINS	The input pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_ENABLEPINS	The enable pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_OUTPUTPINS	The output pins will not be returned from the pins indicated by the 2nd level macro.

Table A-2. Second-Level Exceptions (Continued)

Exception	Result
TmacEX_CLEARPINS	The clear pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_SETPINS	The set pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_RESETPINS	The reset pins will not be returned from the pins indicated by the 2nd level macro.
TmacEX_OTHERPINS	The un-typed pins will not be returned from the pins indicated by the 2nd level macro.

B

Timer Glossary

This glossary defines terms and concepts used in the Timer User's Guide.

clock exception

A terminal in a synchronous network that should be excluded from the specified clock period. The exception can remain undefined (don't care) or can be assigned a unique value in the Path Constraint Editor.

critical path

The path within a design that dictates the fastest time at which an entire design can run. This path runs from the source to a sink node such that if any activity on the path is delayed by an amount *t*, then the entire circuit function is delayed by time *t*.

delay constraint

A delay constraint defines a fixed amount of time required for a signal to propagate from all starting terminals to all ending terminals for a network.

destination

An ending point, sink node, for a timing analysis path, often the data input of a synchronous element or pad.

don't care path

A signal path in which the delay is considered to be infinite.

DTL terminals

Direct Time Layout (DTL) terminals define the starting (or source) and ending (or sink) points for a signal path. They are always I/Os or sequential elements; no intermediate combinatorial element is currently supported as a terminal.

Dynamic Timing Analysis

Dynamic timing analysis (simulation) has been the standard mechanism in verifying design functionality and performance. Both pre-layout and post-layout timing analysis can be performed via the SDF interface. Pre-layout timing analysis provides quick estimates of

the designs performance. Post-layout timing simulation on the other hand provides accurate timing information that is appropriate for device or system level simulation.

filter

A set of limitations or options applied to the timing analysis to more specifically target important items of interest.

global Stop

A defined intermediate point in a network that forces all paths through the defined point to be don't care paths regardless of any constraint assignment.

network

Network. A network can consist of 1 or more start terminals and 1 or more end terminals. All signal paths connecting any start terminal to any end terminal are included in the network. Only one delay value can be assigned to each defined network. Networks can be defined implicitly by a common clock (synchronous network) or explicitly by a defined set of terminals. Network and Paths are used interchangeably.

path

An ordered set of elements identifying a logic flow pathway through a circuit. A path may consist of a single net or a grouping of related nets and components. There can be multiple, or parallel paths (consisting of nets and components) between the two pins. When a component is selected as part of a path, both the input pin to the component and the output pin are included in the path. A path stops when it reaches the data input of a synchronous element (flip-flop) or pad. A path usually starts at the output of a synchronous element or pad.

path delay

The path delay defines the sum of all the individual delays of the nets and the logic macros in the signal path.

path sets

In this manual we refer to groups or categories of paths as “sets.” Path sets are displayed on the Paths tab.

signal path	The signal path describes a consecutive sequence of logic and nets, the first net being driven by a start terminal, and the last net driving a macro input pin of the end terminal
slack	The difference between the constraint and the analyzed value, with negative slack indicating the analyzed value is greater than the constrained value.
Standard Delay Format (SDF)	Standard Delay Format is an industry-standard file format used for storing timing data generated by EDA tools. It is often used for simulation.
Static Timing Analysis (STA)	Static timing analysis is an exhaustive and convenient method of ensuring that the design meets its timing requirements. There are functions that are especially easy to analyze with the static approach. Complex functions such as a multiplier are much easier to analyze using the static approach because static analysis offers one hundred percent coverage with minimal effort compared to dynamic timing analysis. In addition, the static approach is faster for highly synchronous designs compared to dynamic timing analysis.
status bar	The area located at the bottom of an application window

C

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature, Customer Service, investor information, and using the Action Facts service.

The Actel toll-free line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
From Canada, call (408) 522-4480.
From Europe, call (408) 522-4252 or +44 (0) 1276 401500.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Guru Automated Technical Support

Guru is a web-based automated technical support system accessible through the Actel home page (http://www.actel.com/guru/). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations, and links to other resources on the Actel web site.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. The URL is http://www.actel.com.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. We constantly monitor the e-mail account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support e-mail address is **tech@actel.com**.

Telephone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

(408) 522-4460
(800) 262-1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Please see our list of Worldwide Sales Offices.

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