# Verifying Setup and Hold Times in Timing Tools

To verify that a design works properly, both the design's functionality and its timing must be checked. Static timing analysis checks timing, but not the design's functionality. Simulation checks the functionality of a design, but it may miss some timing problems. Used together, static timing analysis and simulation complement each other to provide complete design verification. Various types of simulation tools can be obtained through Computer Aided Engineering (CAE) companies, and static timing analysis can be performed using Actel's Designer Series Software. This application note explains how to create a setup and hold timing report and how to address any timing issues that may arise.

To obtain setup and hold information on a design, first make sure that the design is loaded in Designer and that timing constraints within DT Edit are set on the clocks of the flip-flops. Then from the **Reports** menu of Designer select **Timing…**. The Timing Report options window will appear. From this window, select **Slack** for **Sort By** and click **Preferences**. Within the Preference window, click **Setup-hold Timing Check**, and then click **OK** in both windows.

The displayed report will have information on the device and operating conditions at the top. Below that section will be information on timing for individual paths. The last section of the timing report is a table with a summary of the timing information for setup and hold for each register. For the purposes of this application note, we will focus on this timing information table.

All timing numbers on this report is displayed in slack time. *Slack* is defined as the delay difference between the timing constraints you enter and the actual delay. If a timing path's slack is negative, then the actual delay did not meet the desired timing, missing by the absolute value of the slack delay (in nanoseconds). If the slack value is positive, then the timing constraint was met, with the slack value (in nanoseconds) to spare.

Figure 1 below is a sample design that illustrates what the setup and hold-time table means.

The clock cycles of CLK_1 and CLK_2 are 20 ns and 10 ns respectively.

Figure 2 is the setup and hold-timing information table from the preceding design.

In this example, since all of DDF_1's slack times are positive, it met all of its setup and hold-time requirements. The setup time slack was 0.1 ns which means that the data was valid for that flip-flop with 0.1 ns to spare. The hold-time slack for DDF_1 is 19.2 ns, which means that the flip-flop had 19.2 ns to spare to make its hold time. Finally, the pulse width slack is 4.8 ns, which means that the clock pulse width was larger than the minimum required by 4.8 ns.

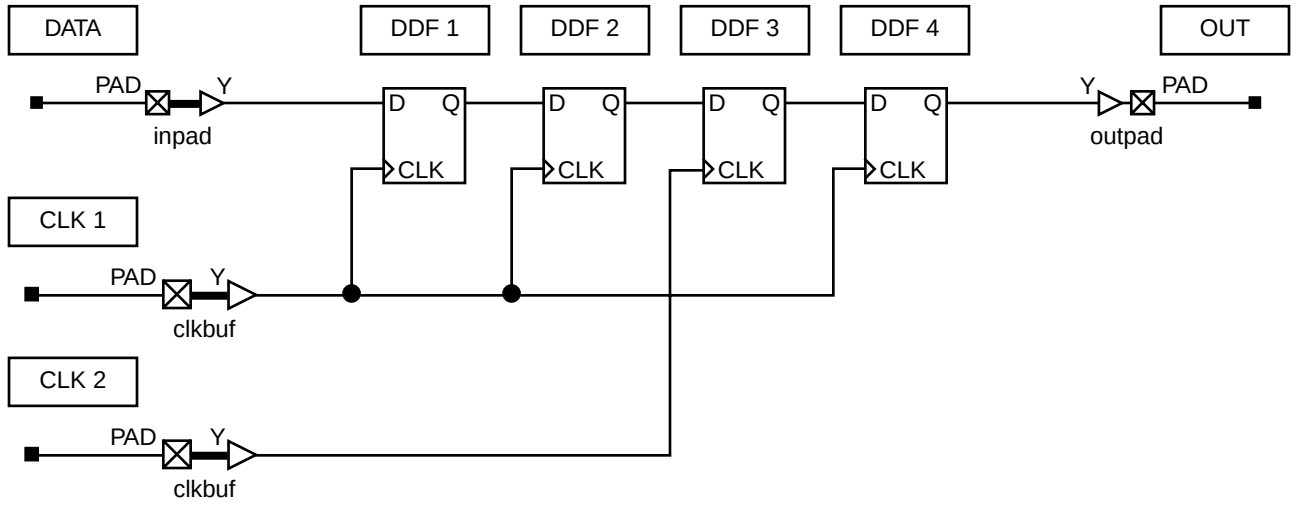


***Figure 1 •*** *Sample Design*

| Slacks for Setup/Hold/Pulse Width Timing Check | | | |
|---|---|---|---|
| Gated Pin | Setup Time(ns) | Hold Time(ns) | Pulse Width(ns) |
| DFF_1:D | 0.1 | 19.2 | 4.8 |
| DFF_3:D | 4.6 | 13.9 | -0.2 |
| DFF_2:D | 14.6 | 3.9 | 4.8 |
| DFF_4:D | 15.0 | -6.1 | 4.8 |

***Figure 2 •*** *Sample Setup and Hold Timing Information Table*

For this example, all of the setup-time slacks for all the flip-flops are positive, which means that all the flip-flops meet setup time. Setup-time slack is calculated by subtracting the longest data time from the shortest clock delay for the corresponding flip-flop. The setup times for the flip-flops can be violated if the clocks run too fast. For example, DDF_3 has a setup-time slack of 4.6 ns, with a 10.0 ns clock period. If the clock period were reduced to 5.3 ns, DDF_3 would have a negative slack of 0.1 ns and its setup time would not be met.

You will notice that DDF_3 has a negative pulse-width slack. This means that the pulse width for the clock on that flip-flop was too small. In this case, it is too small by 0.2 ns. What this means is that for the flip-flop to see the clock as valid, the pulse width for that clock must be increased by 0.2 ns. There are two ways to achieve this. First, you can increase the period of the clock by 0.4 ns. (Given a 50% duty cycle, this will increase the pulse width by 0.2 ns.) You can also change the duty cycle so the high pulse of the clock is 0.2 ns longer. (In this case a 52% high, 48% low duty cycle is required.) But then the negative cycle of the clock will be reduced by 0.2 ns, and you will no longer have a clock with a symmetric waveform.

***Note:*** *If you are using a negative-edge-triggered flip-flop, the pulse width will refer to the negative cycle of the clock. If DDF_3 were a negative-edge-triggered flip-flop instead of a positive-edge-triggered flip-flop, changing the period would fix the pulse width problem. However, the change in the duty cycle would have to be reversed. Instead of changing the duty cycle to 52% high, it would have to be changed to 48% high so the negative pulse would be increased by 0.2 ns (and the positive pulse would be reduced by 0.2 ns).*

DDF_4 has a negative slack for its hold time. This means that DDF_4 did not meet its hold-time requirements. Hold-time slack is calculated by taking the shortest data time and subtracting the longest clock delay for the same clock cycle. In the case of DDF_4, the longest clock delay is the propagation delay from the input of CLK_1 to the CLK pin of DDF_4 (7.8 ns) plus the period of that clock (20.0 ns), which totals 27.8 ns. The shortest data time for DDF_4 is the delay from the previous flip-flop (DDF_3) which is 11.7 ns plus DDF_3's clock (CLK_2) period (10.0 ns), a total of 21.7 ns. The result of subtracting 27.8 ns from 11.7 ns is –6.1 ns, which is the slack. To correct the hold-time problem, either the longest clock delay must be reduced or the shortest data time must be increased. In the case of this example, changing the clock period of CLK_2 from 10.0 ns to 16.1 ns will fix the hold-time problem.

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