Commercial to Radiation-Hardened Design Migration

Introduction

Because the environmental properties of radiation-hardened devices are not required for design prototyping, Actel provides less expensive, compatible commercial devices for this purpose. Although the radiation-hardened devices and the commercial versions are functional equivalents and footprint compatible, they differ in their timing characteristics because of differences in their process geometries. This application note describes design practices that make it easy to verify timing when using commercial devices as prototypes for radiation-hardened devices. Many of these suggested design practices can also improve design completion time.

Good Design Practice

The key to minimizing or eliminating timing problems between device types is to follow good design practice. Good design practice is a design approach that is immune to process and environmental conditions and is easy for timing tools to model. Timing tools can be either dynamic-simulation tools or static-timing tools, which are easier and quicker to use. Actel provides the DTAnalyze static-timing analysis tool with the Designer Series software. The best design practice is fully synchronous design, which allows the timing to be verified with simpler static-timing tools and which makes the design easier to debug and understand.

Fully Synchronous Design

Fully synchronous design has three basic rules:

Rule 1—All register elements that share data should be directly connected to a single common global clock buffer, as shown in Figure 1. Actel provides high-drive, low-skew global buffers for use as clock drivers and for global reset signals.

Rule 2—Every element should be triggered on the same clock edge to eliminate duty cycle issues.

Rule 3—If multiple clocks are required and share data, the data should be resynchronized with one or two registers when changing clock domains, as shown in Figure 2. This ensures that the data will be in a known state.

Fully synchronous design practice is straight forward, but it may lengthen the up-front design time. This time is easily recovered on the back end of the design process, as timing verification can be performed much more quickly. Fully synchronous design practices may use more design resources,

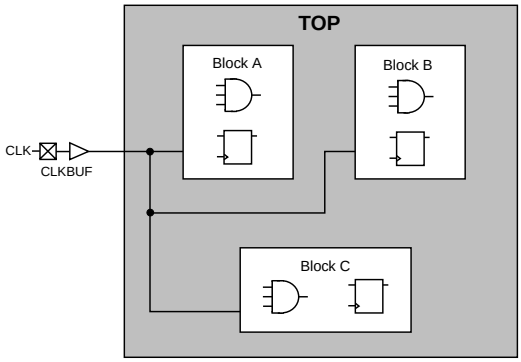


Figure 1 • *A Single Common Global Clock Buffer*

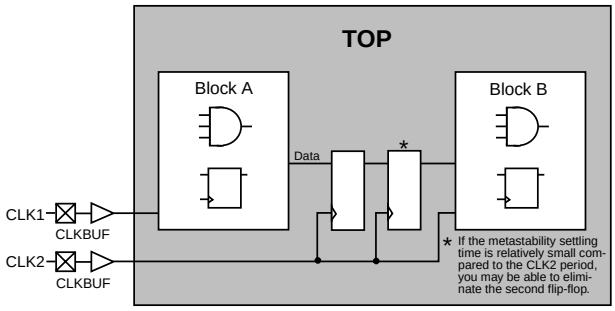


Figure 2 • *Synchronizing Data Between Multiple Clocks*

but the trade-off is in achieving more stable circuits. Other savings in back-end design time can be attributed to the following:

- Shorter debug time. Designs don't take as long to debug because of less complexity, which may make the design more reliable as well.
- Less timing analysis and verification. The timing of fully synchronous designs can be verified using simple static-timing analysis. Poor design practices require dynamic simulation, which requires additional effort.
- Ease of migrating to different process geometries. When migrating from commercial to radiation-hardened devices, timing verification needs to be done again. With synchronous design practices, verification can be done simply by using static-timing analysis rather than timing simulation, which is laborious. This results in time savings both during the prototyping stage and during final design verification.

Common Violations and Corrections

This section describes common violations of fully synchronous design practices, an example of each violation, and a sample "good" circuit. The registers used in the examples are representative only and can be replaced with sequential, combinatorial, or TMR registers. For more information about design techniques aimed at improving the radiation hardness of a design, see the applications note "Design Techniques for RadHard Field Programmable Gate Arrays."

Clock Gating

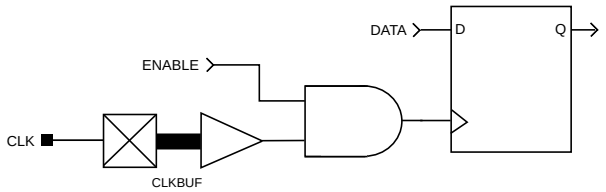
It is possible with the clock gating circuit shown in Figure 3 to produce timing problems that could result in glitches on the clock line. Further, it is difficult to assess the timing of this circuit in relationship to other parts of the design, and using this circuit precludes the use of low-skew global clock buffers

Derived Clock(1)

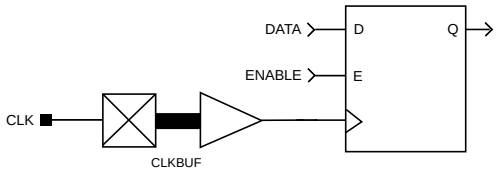
This is a variation of the clock gating problem. The best solution in this case is to use the "clock" signal as a clock enable and to use a global system clock, as shown in Figure 4.

Derived Clock(2)

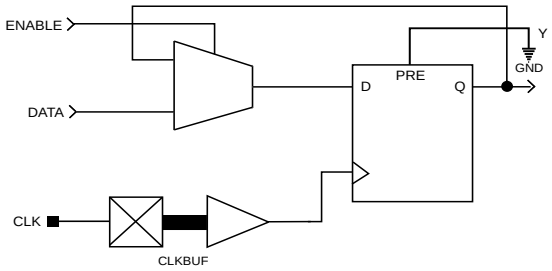
This is commonly used when dividing down the clock frequency. Problems sometimes occur if the data clocked by the lower frequency is merged back into a circuit using the original clock. There might be delay differences, especially if global clock buffers are not used for both clocks, which may make it difficult to analyze the timing. Also, if many different divided clocks are used, you may run out of global clock buffers. As an alternative, consider using instead a clock enable, as shown in Figure 5. This allows the same system clock to be used throughout the circuit, thereby reducing the number of global clock buffers required. The disadvantage to this method is that more routing resources are required, but the speed of the circuit may improve.



Clock Gating Bad Example



RH1020 Sample Good Example



RH1280 Sample Good Example
(using a combinatorial flip-flop)

Figure 3 • *Gate Clocking Examples*

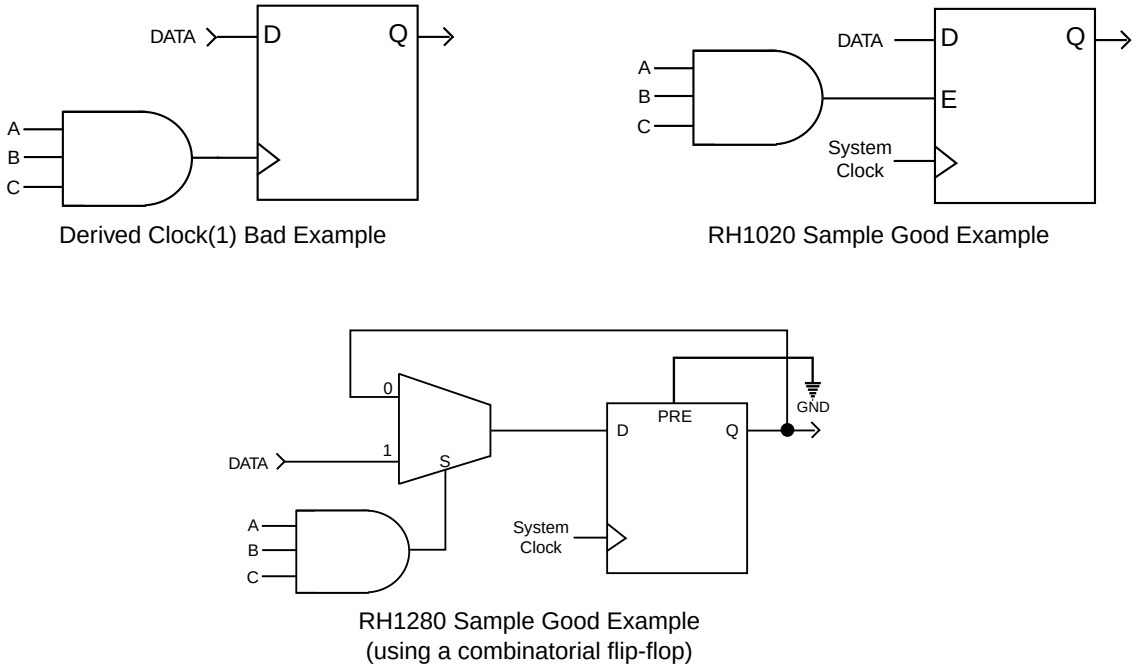


Figure 4 • *Derived Clock(1) Example*

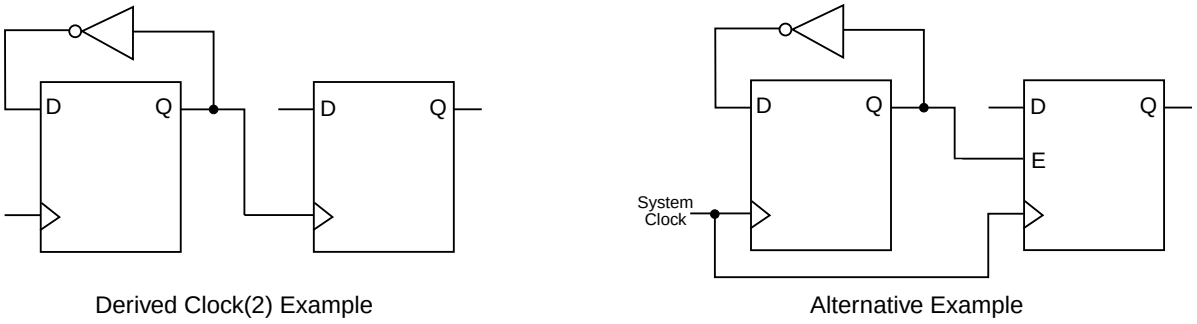


Figure 5 • *Derived Clock(2) Example*

Asynchronous Feedback

The variances in the routing delays make the asynchronous feedback circuit unstable and may result in unexpected functionality. Replace this circuit with a circuit that changes with the clock, as shown in Figure 6.

Asynchronous One Shots

Use of the asynchronous one-shot circut can result in a variant of the asynchronous feedback problem. Use a single system clock to create a synchronous pulse, as shown in Figure 7.

Delay Lines

Due to variances in routing delays and process parameters, the timing of delay-line circuits will vary. Situations that require specific timing should be avoided. If specific timing is necessary, use an external delay-line device outside the Actel FPGA.

Failure to Sample Asynchronous Data

Use of this type of circuit (see Figure 8) is similar to resynchronizing the data when going from one clock domain to another, except that the data is coming from an unknown source, perhaps from off the chip. This is particularly harmful when going into a state machine. Again, use one or two registers to sample the data.

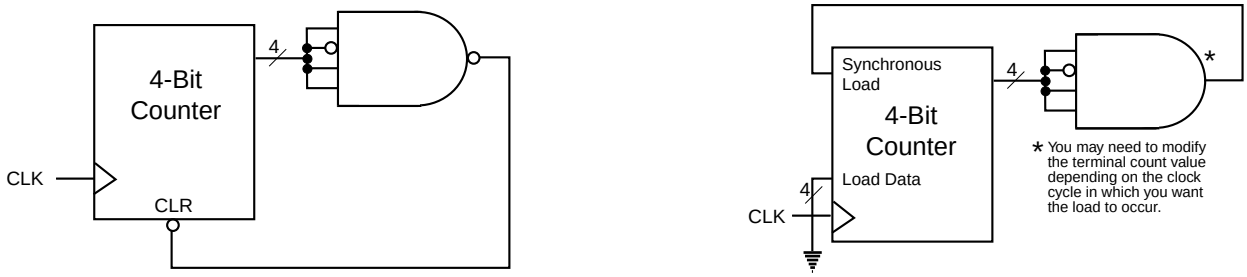


***Figure 6** • Asynchronous Feedback Example*

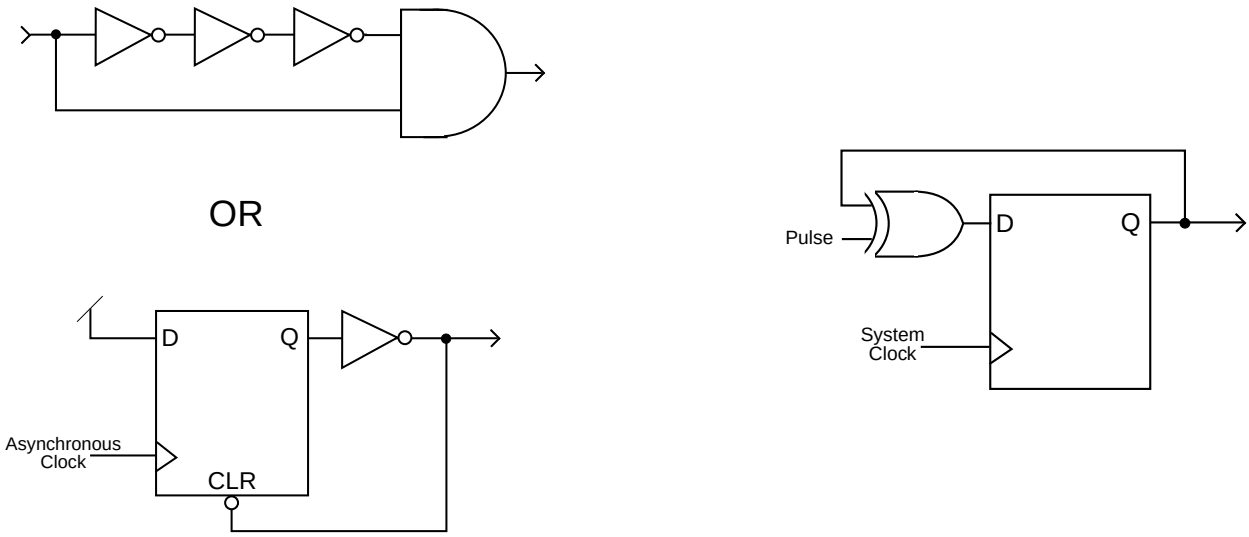


***Figure 7** • One Shot Example*

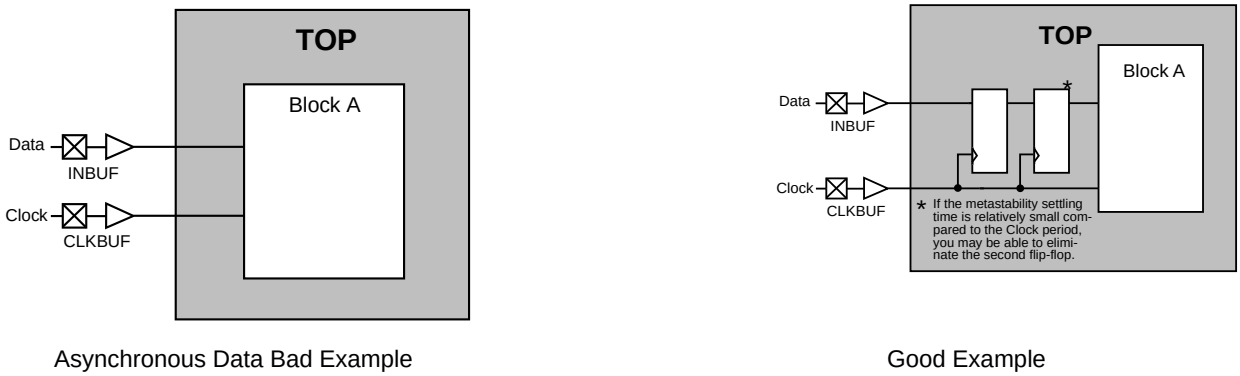


***Figure 8** • Asynchronous Data Example*

Poor Implementation of Synchronous Preset/Clear

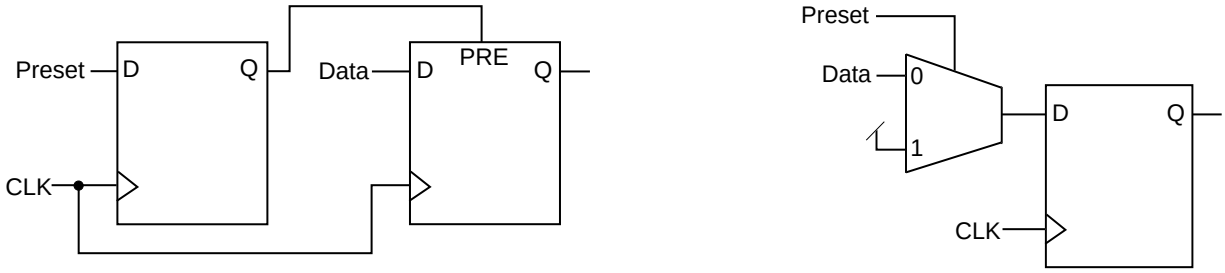
The "poor" implementation shown in Figure 9 has potential metastability problems. Don't try to preset (or clear) and clock a flip-flop with the same clock edge.

Conclusion

Synchronous design techniques make it easier to migrate to radiation-hardened devices when using less expensive commercial parts as prototypes. Doing synchronous design is straightforward and can save overall design time by reducing the time it takes to perform timing verifications and by reducing the complexity of the design.

For additional information about designing when using radiation-hardened devices, visit the following web site:

http://www.actel.com/products/radhard.html



Poor Synchronous Preset Example

Good Example

Figure 9 • *Synchronous Preset Example*

Take it to a higher level.

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