Actel®

eZone single-chip FPGA news

Summer 2007

innovative power smart solutions


**Since the 1990s, the concept of power has greatly changed. No longer simply about supplying power, "power" encompasses power consumption and energy conservation as well as low-power ICs, fab processes, regulators and chargers.**

Though companies are talking about reducing power consumption and energy usage across the power continuum, not enough has been done. In eZone, read about Actel's range of innovative power-smart solutions, including the ultra low-power 5 µW IGLOO™ FPGA family and Fusion PSCs for power management.

## Accelerating Design Entry with Libero® IDE v8.0

Faster design creation + Fewer design errors = More designs in less time

With the release of Libero Integrated Design Environment (IDE) v8.0 Actel introduces SmartDesign to further ease the system-level design process when using its FPGAs and underscores its commitment to deliver and support power-efficient solutions. **Find out how SmartDesign** can accelerate design using Actel IP, Processors and Analog Systems together in a single design view.

### THIS ISSUE



## Actel News

June 25, 2007 Actel Launches Low-Power RTAX-SL FPGAs for Space Applications

May 25, 2007 Actel Discusses Power Management in Platform-Based Systems at the MicroTCA Summit

May 14, 2007 Aldec Delivers Prototyping Solution for Actel RTAX-S Space FPGA Designs

Apr 06, 2007 Actel IGLOO Family Wins Prestigious 2007 EE Times ACE Award

Apr 03, 2007 Avnet And Actel Chosen for General Vision's Image Recognition Solutions

**Read the New Power-smart White Paper**

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*Actel Corporation is the leader in single-chip FPGA solutions.*

ONE CHIP is all you need

## John East » View Point

### Getting Ahead of the Power Curve

Today, the way we interact, inform and communicate is increasingly electronic. Unfortunately, generating the electricity required to power electronic systems contributes to a surprisingly high fraction of the greenhouse gasses associated with global warming. Recent predictions, based on those gasses, suggest that average global temperatures will rise by as much as eleven degrees Fahrenheit by the turn of the century.

**This is a problem!**

As we absorb this reality, companies are talking about reducing energy usage. However, for the electronics industry, taking responsibility is no longer a choice. It is mandatory. To get ahead of the power curve, we must address energy consumption across the continuum – from chips to systems.

In the industry, we are seeing growing availability of low-power chips, which have been designed to reduce power consumption with minimal performance impact. Also important are user-friendly flexible implementation options or modes to further reduce total system power when the system is idle. Actel is leading the charge with our range of power-smart solutions, including our ultra low-power 5 µW IGLOO FPGA family and our Fusion PSCs for power management.

Similarly, from a system perspective, we need to make systems smart enough so they don't consume power if they don't need to. Smart enough to know how much power they're using and why. Smart enough to recognize problems and provide solutions. By enabling system-level solutions for ATCA, MicroTCA, IPMI and other standards, Actel's power-smart, mixed-signal Fusion technology will aid in the management of the system's power environment.

As the world becomes more electronic, the electronics industry needs to focus on reducing energy usage in all parts of the power continuum. At Actel, we have placed great emphasis on developing and delivering innovative, power-smart technologies to address the power problems facing today's designers.

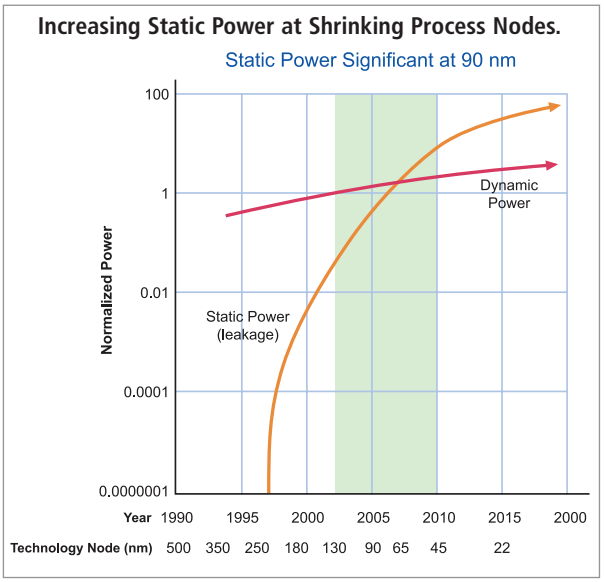
***Together, we can get ahead of the power curve.***

**John East**
President and CEO, Actel Corporation

# Are you a Power Smart Engineer?

**Power in semiconductor devices takes two basic forms – static and dynamic. Static power is consumed when the part is doing no useful work, while dynamic power is consumed when devices are actively working.**

Until recently, dynamic power has been the dominant source of power consumption. In the past reduction of dynamic power has come from process shrinks and lower system voltages, but it seems we have reached the point of diminishing returns. With smaller process geometries, worsening leakage current, causes static power to dominate the power consumption.




Now that the somewhat "easy" power gains of shrinking process have passed, we have the opportunity to find ever more creative ways to cut power. It is no longer up to just the semiconductor designer to create the power gains, but up to each engineer to choose technology that allows better power choices at each level of design. Choosing the lowest power FPGA or choosing a device with built-in smarts to allow your system to manage power, becomes another level of learning for the ever evolving design engineer.

## Low Power Devices

Designers of portable, battery-powered equipment are faced with a daunting challenge – insatiable consumer demand for smaller, cheaper, feature-rich portable devices, with longer battery lives, lower cost and short time to market. If the battery life of a smart phone is good for six hours and if lithium ion batteries typically support 300-500 recharge cycles, before a "costly" battery replacement is required, wouldn't these devices be even more attractive if the battery life was extended beyond six hours to weeks or months?

Compared with today's "low power" best-of-breed SRAM-based FPGAs, Actel's flash-based IGLOO FPGAs deliver between one hundred and one thousand times improvements in power consumption.
Read more about IGLOO FPGAs opposite.

## Power Smart Systems

Power-smart chips offer more than just low-power consumption. They can be used to intelligently control and reduce total power consumption in the overall system. For example, the mixed-signal Actel Fusion™ Programmable System Chip (PSC) offers the integration of FPGA logic with other elements used in system management, such as flash, analog, microprocessors and clock management. This integration enables designers to remove parts from the board, reducing total power consumption and bill of materials (BOM) costs, and enabling sophisticated power management of the system.

An off the shelf, flash-based, single-chip, field-programmable device implementation allows the designer to create a simple and inexpensive system management solution.

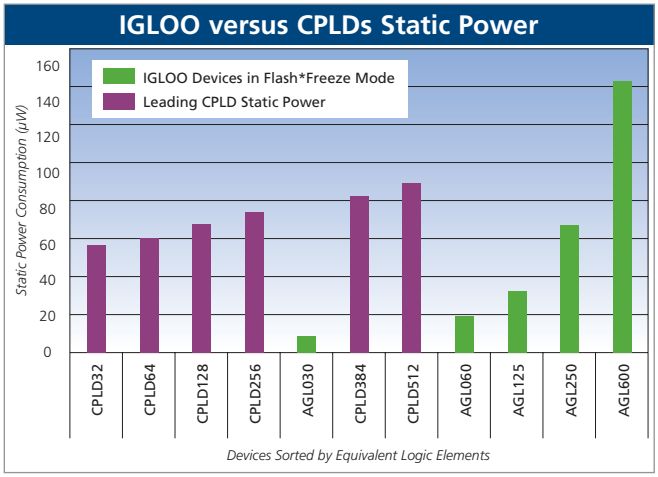
Read more about Fusion PSC usage on pages 4 and 5.

# IGLOO 5 µW FPGAs

## – *the Smart Choice for Low Power*

IGLOO™ With Flash*Freeze

**Compared with industry-leading low power CPLDs, IGLOO FPGAs, with static power as low as 5 µW, deliver more complexity and features than CPLDs, with four times lower static power and as much as five times longer battery life in portable applications.**




Then compare with today's "low power" best-of-breed SRAM-based FPGAs, Actel's flash-based IGLOO FPGAs deliver between one hundred and one thousand times improvement in power reduction. This two to three orders of magnitude lower static power consumption can translate into weeks and months of standby battery life. Use the Power Calculator or SmartPower links to see how IGLOO will perform in your design.

**Analyze Your Power Modes on IGLOO Power Calculator**

actel.com/eZone/IGLOOcalc

**Test Your Design in SmartPower**

actel.com/ezone/SmartPowerTEST


**Learn about 5 µW FPGAs View Webcast**

actel.com/support/webcasts

## Flash*Freeze

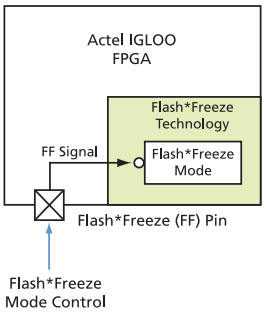
**The IGLOO device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly enter and exit Flash*Freeze mode, within 1 µs, by activating the Flash*Freeze pin while all power supplies are kept at their original values.**

- I/Os and global I/Os can still be driven and can be toggling without impact on power consumption
- Clocks can still be driven or can be toggling without impact on power consumption
- Internal clocks from PLLs are automatically disabled
- Device retains all core register, SRAM information, and states
- I/O states are tristate during Flash*Freeze mode or can be set using weak pull-up or pull-down attribute
- No power is consumed by the I/O banks, clocks, JTAG pins, or PLL
- IGLOO devices consume as little as 5 µW in this mode.

### Flash*Freeze Usage type 1

*In Flash*Freeze mode type 1, entering and exiting the mode is exclusively controlled by the assertion and de-assertion of the FF pin.*

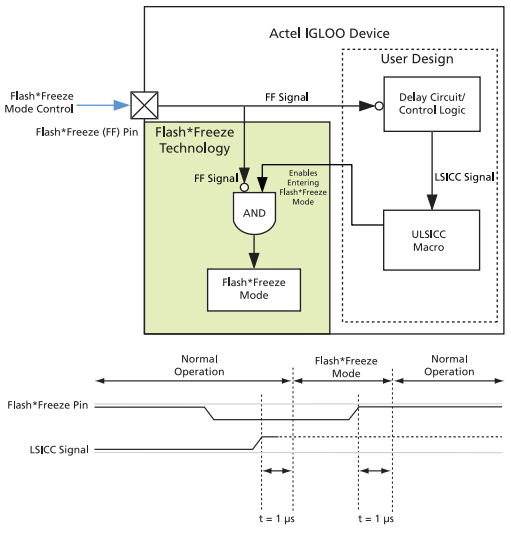
The device will enter Flash*Freeze mode 1 µs after the dedicated FF pin is asserted, and returns to normal operation when the FF pin is deasserted. This mode is implemented by enabling Flash*Freeze mode (default setting) in the Actel Designer software. The FF pin threshold voltages are defined by $V_{CCI}$ and the supported single-ended I/O standard in the corresponding I/O bank. The FF pin has a built-in glitch filter that ensures spurious glitches are filtered out to prevent entering or exiting Flash*Freeze mode accidentally.




### Flash*Freeze Usage type 2

*In Flash*Freeze mode type 2, entering and exiting the mode is controlled by both the FF pin AND the user-controlled logic.*

The device can enter Flash*Freeze mode by activating the FF pin together with other user-defined control logic or delay circuitry within the FPGA core. This method enables the design to perform important activities before allowing the device to enter Flash*Freeze mode, such as transitioning into a safe state or completing the processing of a critical event. The device will only enter Flash*Freeze mode when the Flash*Freeze pin is asserted and the ULSICC macro input signal, called the LSICC signal, is asserted.




## Fusion Architecture Webcast

Discover How the Fusion Family's Front-End and Flash Memory Enable a Host of Power Management Applications

## Fusion Design Flow Webcast

Learn How Actel Simplifies Mixed-Signal FPGA Design

**actel.com/support/webcasts**

# Fusion Starter Kit

**This all-inclusive, low-cost Starter Kit, contains everything needed to use the advanced features of Actel Fusion.**

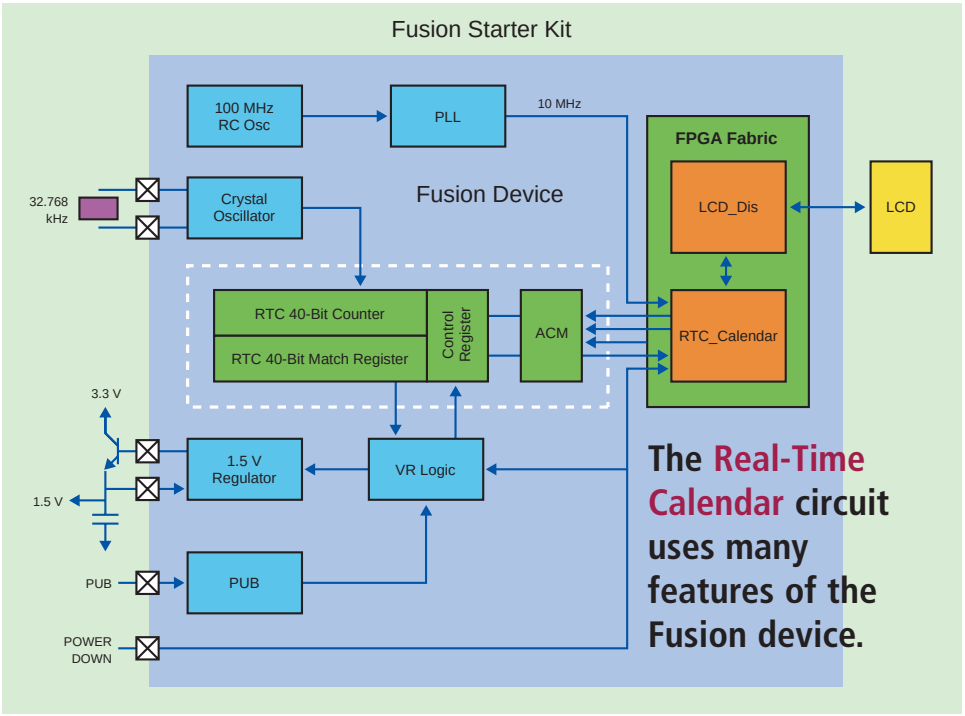

The Evaluation Board hosts the AFS600-FG256 device, with selectable voltage sources, LCD display, prototyping headers, and a 40-pin daughter card connection. It comes with FlashPro3, an in-system programmer, Libero IDE Gold "which supports all Actel devices up to 1 M system gates" and a User's Guide, tutorial schematics, and design files.

# Real-Time Calendar

## *for Portable or Managed Power Applications*

**A Real-Time Calendar can be used for an alarm clock, data logging, or any applications that require time and date stamp information.**

By combining the Calendar with Fusion, you can control the power and operation of your entire system for power cycle timers etc. Actel Fusion™ is the world's first mixed-signal FPGA, integrating configurable analog, a real-time counter (RTC), flash memory blocks, and clock generation circuits—all in a single chip. Fusion can be used to manage power sequencing and ramp-rate for all supplies in your system. Using the Fusion device's RTC, this application provides a count of seconds, minutes, hours, day of the week, day of the month, month, and year. The month-ending date is automatically adjusted for months with less than 31 days, including corrections for leap years. Moreover, the FPGA core can be turned off to save power, and the RTC will continue to keep track of the time and date information.




**Using a 32.768 Hz crystal oscillator, with built-in prescaler, provides a 256 Hz input to the Real-Time Counter, which gives the 8th bit a 1 Hz frequency. The 40-bit counter can count for over 136 years.**

A single 3.3 V supply into the device drives the 1.5 V regulator, which is used to power the FPGA logic. The regulator can turn off power to the FPGA core with the RTC still running, so it can continue to track time until the device wakes up. For low-power applications, the Fusion device with crystal oscillator and RTC running pulls approximately 200 µA. The device can be signaled to wake up from an external trigger through the PUB pin or from a match being reached within the counter.

A reference design is described in the *Real-Time Calendar Applications in Actel Fusion Devices* application note. The design files can be downloaded for use with the Fusion Starter Kit, which provides source code for an example using an external trigger for power-down and restart. This design could be modified to show automatic wake-up when a preset time is reached. Data and timestamp information can be written and stored in the embedded flash while the device is powered down.

In addition, the design includes LCD driver code for use with the starter kit to display date and time.

**For App Note and Design Files visit: actel.com/ezone/RTC**

# Power Sequencing and Ramp-Rate Control in a Mixed-Signal PSC

**With increasing complexity of board-level power supply management and the need for adjustable power-up sequencing and ramp-rates, designers need a flexible system management master.**

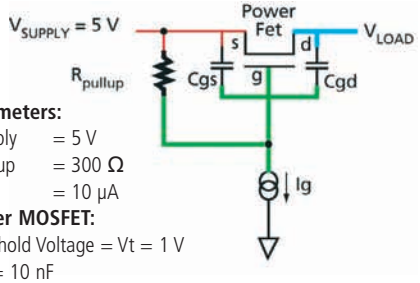
Generating and maintaining the appropriate power environment is critical to proper system operation.

Designs with FPGAs, DSPs, and ASICs can demand four, five, or even more power supplies to power up in a prescribed sequence and ramp-rate, in order to avoid issues such as latch-up, inrush current, or I/O contention. Fusion, with its analog quad, analog I/O structure and analog-to-digital converter, represents a smart, simple, and flexible solution for power sequencing and ramp-rate control.

**Power Sequencing** may require several different approaches:

- A fixed delay between supplies
- A second supply starting after a minimum threshold is reached on the first.
- Multiple supplies with different ramp-rates
- Synchronous ramp-rates to 2 final different voltage levels

### Ramp-Rate Control




**Parameters:**
Vsupply = 5 V
Rpullup = 300 Ω
Ig = 10 µA
**Power MOSFET:**
Threshold Voltage = Vt = 1 V
Cgs = 10 nF
Cgd = 2 nF

For a given power supply voltage, Ig and Cgd define how soon it can ramp up to its full scale, based on the following: **dV/dt = Ig/Cgd**

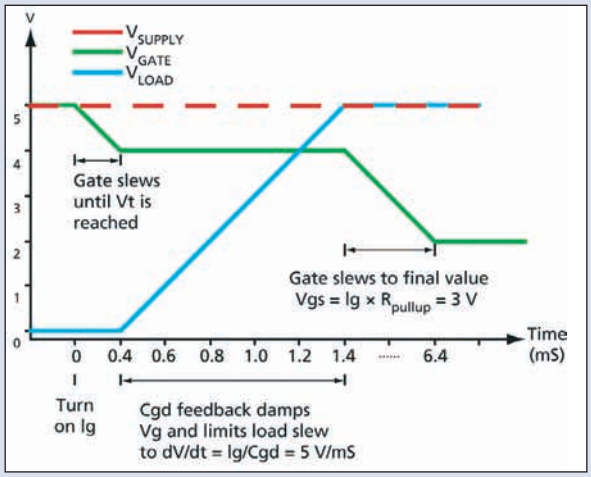
**Ig** = *Drive strength of the Fusion gate driver, or source/sink current on the gate, selectable in Fusion from 1 µA, 3 µA, 10 µA, 30 µA.*

**Cgd** = *Parasitic capacitor between gate and drain of the power MOSFET transistor.*

## Example

In this example, the supply voltage is on before time 0. When the Fusion gate is turned on the Voltage on the gate slews until Vt is reached; then the load side will show the smooth ramp-rate of 5 V/ms from 0 to target, based on the calculation below.
**dV/dt = Ig/Cgd = 10 µA/2 nF = 5 V/ms**

Once the target voltage is reached, the gate slews to the final value determined by the following equation:
**Vgs = Ig x Rpullup = 3 V**




The selection of the MOSFET must be done with care and knowledge of system requirements. Care must be taken also when selecting Rpullup. If the Rpullup is too large, then the Vgs rating of the MOSFET could be exceeded, leading to catastrophic failure.

**Fusion for power sequencing and ramp-rate control.** Fusion not only provides the ability to control power sequencing and ramp-rate, but the parameters are programmable and reprogrammable in-system, to allow for system adjustment or calibration during test. With temperature, current monitoring, and nonvolatile memory (NVM), the Fusion device is capable of full system management, data logging, and remote communication. *Refer to the webcast for more information on Fusion capabilities.*

**For App Note and Design Files visit: actel.com/ezone/FusionPowerSeq**


### On-Demand System Management and MicroTCA Webcast

Describes how Fusion can be used to integrate system management and Actel's commitment to deliver free MicroTCA reference designs.

**actel.com/support/webcasts**

Download System Management Guide and Register to Win System Management Developer's Kit

**actel.com/ezone/SystemMgtreg**

## Jasper Electronics Uses Actel MicroTCA Reference Platform

Further enabling the growth of the MicroTCA market, Jasper Electronics has developed a MicroTCA power supply, using Actel's MicroTCA Power Module (PM) reference platform. Based on the Actel Fusion Programmable System Chip (PSC), the platform enables the rapid deployment of systems based on the MicroTCA specification.

"In order to take advantage of the rapidly expanding MicroTCA market opportunity, we need silicon providers who are committed to delivering highly integrated, cost-effective solutions that meet the requirements of the standard," said Robert Nishimoto, president, Jasper Electronics. "Not only is Actel the only silicon provider to offer a MicroTCA reference platform, but they also uniquely integrate mixed-signal capabilities and reliable flash memory on a single chip. This innovation has enabled us to dramatically reduce our bill-of-materials cost and offer customers a low-cost, highly reliable power module for immediate integration into their MicroTCA systems."

# Accelerating Design Entry with Libero IDE v8.0

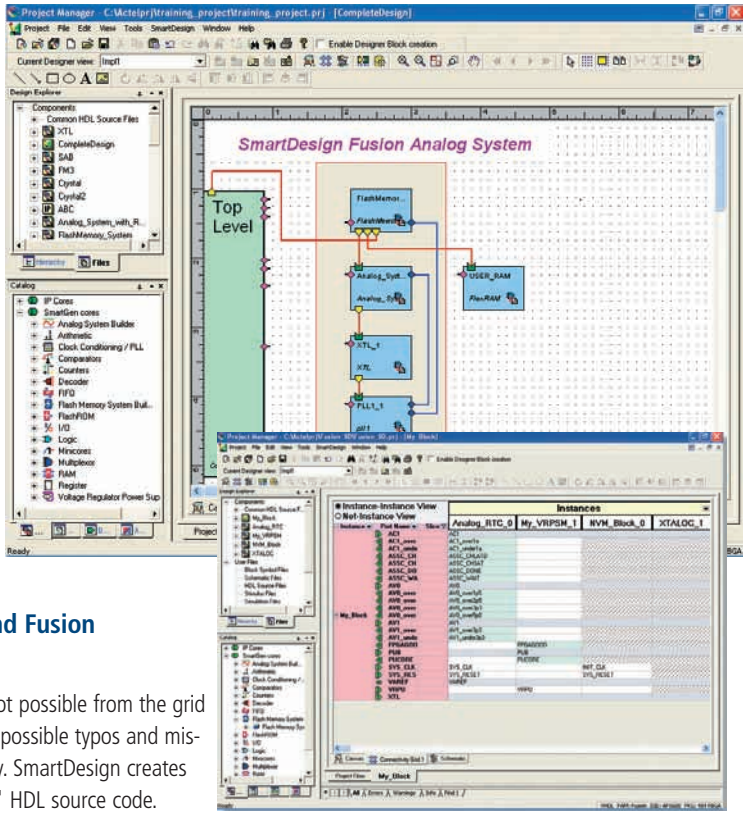
**In the FPGA space, time-to-market is always a key factor. It is one of the reasons to use an FPGA instead of an ASIC.**

It has become the standard for FPGA vendors or third parties to create IP, solutions, and reference designs to get you through your design process as quickly as possible. Building your design often becomes a jigsaw of different formats, tools, blocks, and styles working together.

**Within the Actel portfolio alone, there are multiple options:**

- **SmartGen** cores are configurable standard blocks as well as Fusion design elements.
- **IP Catalog** gives access to over 100 industry-standard functions, either from Actel or third-party suppliers.
- **CoreConsole** can create a processor IP with subsystem to drop into your FPGA fabric.

## SmartDesign




### SmartDesign Canvas

SmartDesign allows you take design elements from the options mentioned above and drop them onto one Canvas, bringing them all into the same playing field. Instead of trying to create and navigate through all the VHDL port maps and connections, you can drop the blocks in and then use the Connectivity Grid to create all your connections. Best of all, you can automatically export a completed VHDL or Verilog file to use at the top level of your design. Fusion analog system and bus interface connections can be made by SmartDesign automatically.

It is presumptuous to assume that your entire design is done for you as a simple jigsaw, so take your own HDL blocks, add them to the Hierarchy, and drop them onto the Canvas to interface with the standard blocks.

### Connectivity Grid

For other device connections, a connections grid displays the blocks in a matrix layout, where intersecting cells become "connection opportunity" points. Pull-down menus display available ports where selections can be easily made and then visually verified.

### Schematic View

Connections on the Canvas are simplified to keep the view clean, but the Schematic view allows you to see all the connections, providing a good sanity check of what you have been working on.

### Design Checking and Fusion Design Assistance

Illegal connections are not possible from the grid intersections, preventing possible typos and mis-connects of manual entry. SmartDesign creates "correct by construction" HDL source code.

SmartDesign understands core dependencies to other cores and busses in Fusion designs, and provides menus and descriptions that allow you to quickly and easily determine the correct solution. SmartDesign then automatically connects the blocks. With SmartDesign's understanding of Fusion Analog and Memory System Builders and auto-connections, plus visual presentations, connections, and verifications performed using the Connectivity Grid, Canvas, and Schematic views, using SmartDesign greatly reduces your design time and eliminates errors.

**For SmartDesign visit: actel.com/ezone/smartdesign**

# Using DDR Interface with Actel's Flash FPGAs

**Double-data-rate (DDR) interface in Actel devices provides a migration path from single-data-rate (SDR) memory interface to a faster interface for enhanced applications.**

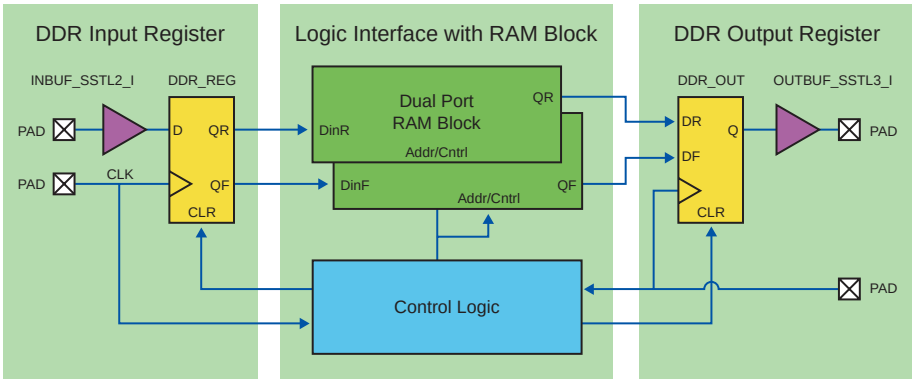
DDR memory interface doubles the bandwidth of the device without increasing the clock speed or bus width. DDR SDRAM provides a source-synchronous data capture at a rate of twice the clock frequency. These devices utilize 2n-prefetch architecture where the internal data bus is twice the size of the external data bus.

The core of a DDR interface is similar to an SDR interface with identical address and control, bank structures, and refresh requirements. The main difference between DDR and SDR interfaces is in the actual data interface. SDR is fully synchronous using the positive edge of the clock. DDR is true source-synchronous and captures data twice per clock cycle.

**Summary of enhancements for DDR:**

- **DDR utilizes a differential pair for the system clock**
- **Data is transmitted on both positive and negative edges of the clock**
- **SSTL-2 signaling is used**

**A good example of using DDR I/Os is in an application where the FPGA is reading data from an external memory, an FPGA, or another external device.**




The data enters the FPGA through a pad and is captured into a DDR register, which splits the data into two outputs: QR and QF. QR is the output at the rising edge of the clock and QF is at the falling edge of the clock. The data is registered into a dual-port SRAM in Actel's ProASIC®3 FPGA. Control logic circuitry is used to control the address space to write data coming from DDR I/O registers to SRAM blocks inside the FPGA for internal processing.

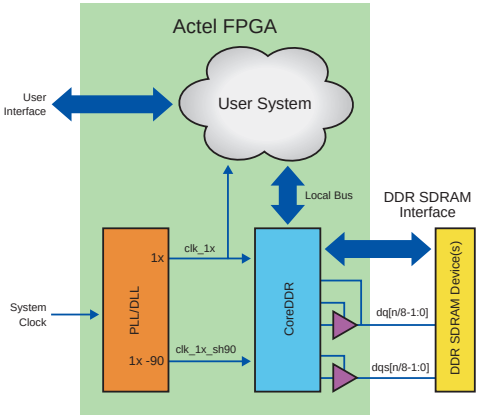
Simultaneously, the data can be sent from an SRAM block through an output DDR register to an external device in the same clock cycle. This doubles the speed of the data throughput into the FPGA, as compared to SDR, where each bit is captured and registered at every clock edge. With this technique, multiple bits of data can fill several addresses of RAM in fewer cycles. Similarly, the data can be sent to an upstream device via an output register and reduce the total number of pins used.

Actel provides reference designs and a development board that is used to demonstrate the communication path from a PCI bus to external DDR memory. To learn more about the DDR memory interface in Actel's flash-based FPGA, visit http://www.actel.com/documents/PA3_E_DDR_AN.pdf.

**Register to Learn about new IP Cores as they become available.**

**www.actel.com/updates**

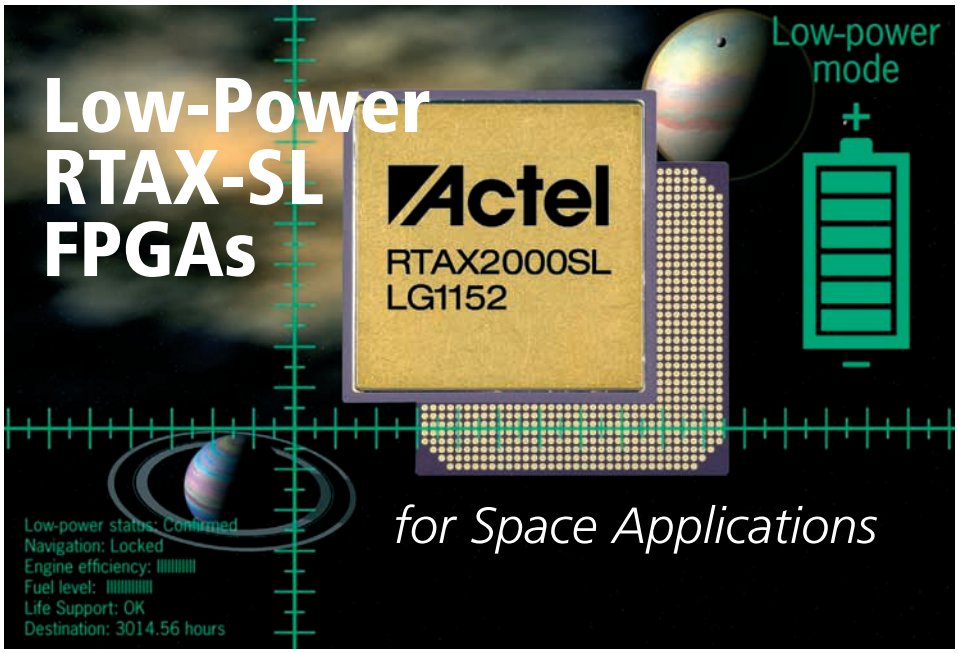
## Actel's DDR SDRAM Controller




- Supports up to 1,024 MB of memory
- Synchronous interface
- Runtime configurable timing parameters
- Bank management logic
- Up to 8 chip selects
- Automatic refresh and initialization
- Supports Fusion, ProASIC3/E, Axcelerator®, RTAX-S

**Register to Learn about CoreDDR**

**actel.com/ezone/CoreDDR**




**Extending its low-power offerings to the space community, Actel has developed the radiation-tolerant RTAX-SL low-power grade option field programmable gate array (FPGA) specifically targeted at high-reliability space-flight designs.**

The industry's lowest-power, programmable logic solution for space applications, the new RTAX-SL option offers approximately 50 percent lower standby current than the leading space FPGA offering at 125°C. Based on Actel's successful RTAX-S architecture, the new RTAX-SL option is comprised of three devices: RTAX250SL, RTAX1000SL, and RTAX2000SL.

Actel® SPACE FORUM

**Actel Space Forum is an interactive one-day user forum featuring in-depth technical presentations, product demonstrations, and a roundtable session presented by technology experts from Actel on how to design effectively with the Actel space products.**

The event also includes roadmap discussions on products, hardware and software tools, and presentations from Actel Strategic Partners such as Synplicity®, Mentor Graphics®, Aldec, Linear Technology, and Gaisler Research on products that support Actel space FPGAs. Customers attending this event will understand and gain knowledge on how to optimize their space applications using Actel FPGAs for performance and power. Actel Space Forum is currently in its third year and is rapidly expanding into an international showcase for Actel space-based solutions. For Information and Reservations Visit: actel.com/asf

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