Actel®

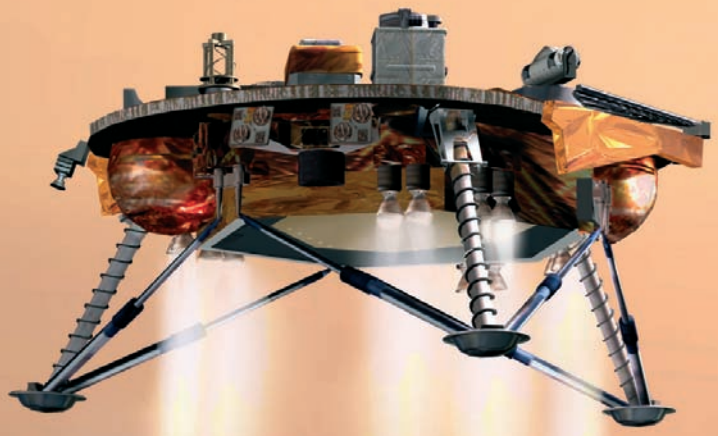
eZone single-chip FPGA news

SPACE EDITION 2007

innovative programmable logic solutions

Phoenix Has Launched!

With RTAX-S On Board



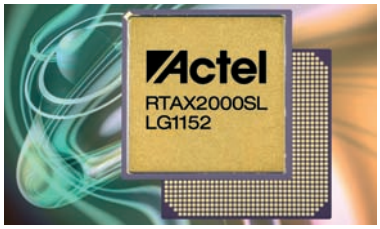
On August 4, 2007, at 5:26 EDT, the Delta II Rocket carrying the Phoenix Mars Lander lifted off from its launch pad at Cape Canaveral Air Force Base. Phoenix will land on the northern plains of Mars and will dig into the soil and water-ice, looking for evidence of past habitability.

Learn about the Phoenix Mission and Actel's RTAX-S Devices.

Actel Reliability and Low Power

"We have a stringent review and evaluation process for our suppliers. Following this review, we determined that the RTAX1000S-CQ352 provided the high reliability and stringent low-power metrics required for this mission-essential function. Using the high-density RTAX-S Actel device, MDA's MET instrument temperature and pressure subsystem is designed to provide accurate data throughout the mission, without failures."

Andrew Kerr Program Manager for the MET program at MDA



RTAX-SL Low-Power Grade

For Space Applications

The industry's lowest power programmable logic solution for space applications, the new RTAX-SL option, offers approximately 50 percent lower standby current than the leading space FPGA offering at 125ºC. Learn more about RTAX-SL.

THIS ISSUE

Actel News

Aug 06, 2007 Historic Phoenix Mars Mission Flies Actel RTAX-S Devices

Jun 25, 2007 Actel Launches Low-Power RTAX-SL FPGAs for Space Applications

May 14, 2007 Aldec Delivers Prototyping Solution for Actel RTAX-S Space FPGA Designs

Nov 21, 2006 Actel's RTAX-S Device Family Hits Major Reliability Milestone

Nov 06, 2006 Actel and Aldec Partner to Offer High-Reliability Design Solutions for Aerospace and Avionics Markets

Sep 18, 2006 Actel and Gaisler Research Soar with RTAX-S Aerospace Microprocessing

Rich Brossart's Comment

RTAX-S

"Our new low-power RTAX-SL FPGA family directly addresses the demand from the space community for lower power solutions as design requirements and power budgets tighten. For high-reliability, mission-critical aerospace systems, our new low-power family, prototyping options, and EV-processing flow enable our customers to reduce system power and save development costs while still meeting the stringent quality and reliability requirements for flight."

Rich Brossart
Vice President of Product Marketing
at Actel Corporation

Prototyping for RTAX-S and RTAX-SL Application Note

Download now

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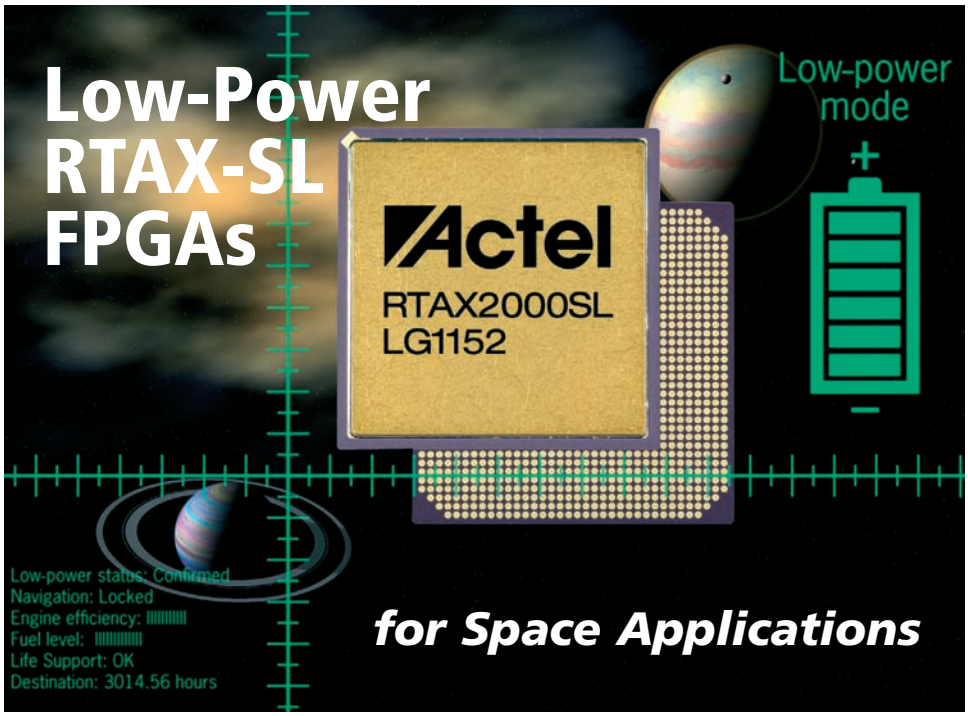


Extending its low-power offerings to the space community, Actel Corporation has developed the low-power, radiation-tolerant RTAX-SL FPGA option, specifically targeted at high-reliability space-flight designs.

Based on Actel's successful RTAX-S architecture, the new RTAX-SL option is comprised of three members: RTAX250SL, RTAX1000SL, and RTAX2000SL. The industry's lowest power programmable logic solution for space applications, the new RTAX-SL option offers approximately 50 percent lower standby current than the leading space FPGA offering at 125ºC. The previous leader was, of course, Actel's RTAX-S devices.

Designed to offer radiation performance that exceeds the requirements of most space applications, the RTAX-SL option also offers embedded memory, SEU-hardened flip-flops, high I/O count, multiple I/O standard support, and hermetic packaging.

Prototyping Solutions for RTAX-S

Delivering Low-Cost Methodology for Validation

Actel provides a comprehensive prototyping portfolio for its aerospace customers. Prototyping options for RTAX-S devices can be classified into three types, described here.

Early Concept Proof – Reprogrammable Flash-Based Devices

For early concept proof of Actel's space-optimized devices, Aldec offers a prototyping solution using Actel's ProASIC®3 flash-based FPGAs, allowing customers to tap the flexibility and reprogrammability of flash-based prototypes for multiple aerospace applications. This is described further on page 7, with links to additional resources.

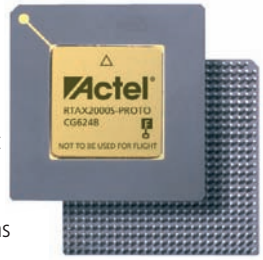
Mid-Level Prototyping

For a cost-effective mid-prototyping solution, Actel offers commercial footprint-compatible Axcelerator® (AX) products with prototyping adaptors. Since RTAX-S/SL devices are derived from the Axcelerator family, the basic architecture remains the same, allowing Axcelerator to provide a functional representation of the RTAX-S device at significantly reduced cost.

Final Verification

Customers at the final verification stage have access to pin-compatible RT silicon with the same architecture, functionality, and timing attributes as the flight-qualified FPGAs.

For full timing verification of RTAX-S/SL designs, customers can use the equivalent PROTO units to validate their flight design. PROTO units provide guaranteed functionality over the full military temperature range. They must not be used for space-flight or other applications that require the quality of space-flight units, such as qualification of space-flight hardware.



The PROTO units are NOT processed or tested to any of the process flows that are offered with the flight units. They are marked, "NOT TO BE USED FOR FLIGHT", as shown on the above package.

These solutions offer tremendous savings in design time by eliminating design cycles, which translates into overall lower development costs.

To learn more about RTAX-S prototyping, visit: actel.com/ezone/space07

Carefully Managing Both Commercial and Space Requirements and Concerns

Some of today's leading-edge research comes directly from the space community.

To best serve this market, the electronics community must carefully balance existing trends and requirements in the commercial market with the needs and concerns of aerospace designers. This is of particular importance as space designers are turning more to commercial parts in response to a diminishing space electronics supply base.

For example, power consciousness is top-of-mind in commercial electronics. Space customers benefit as work to establish lower commercial power consumption carries over to space design. Certainly, power consumption from terrestrial power sources is not as critical as power consumption in space due to the spacecraft's restrictions on solar panel size, nuclear power source, or size and weight of power supply components, thus limiting power budgets. Offering low-power consumption in addition to critical radiation tolerance, Actel's new RTAX-SL FPGA is an example of the careful balancing of commercial trends and aerospace requirements.

Another issue facing space designers is product obsolescence. Often, the product lifetime of today's build-to-print space system exceeds the lifetime of the commercial ICs, meaning that the devices may have passed end-of-life (EOL) while the system is still in production. In order to avoid an expensive and time-consuming design update and system requalification, the manufacturer has to scramble to acquire the EOL devices from whatever sources are available.

By their very nature, FPGAs are a great silver bullet in the battle against component obsolescence. Instead of redesigning the system using a more recent version of the EOL device, which could also face EOL, designers can target FPGAs, thereby reducing cost and eliminating respins and requalifications. With FPGAs, designs can also be ported to next-generation technology with improved performance, lower costs, and new features and capabilities.

Actel has a long and respectable history of providing programmable solutions to the space community. Actel continues to develop products that carefully balance commercial issues with the challenges and requirements of emerging space applications, including in-flight or in-orbit power consumption. Actel is also committed to maintaining its industry-leading product lines, such as the RTSX-SU and RTAX-S families, as long as possible to aid our customers' success.

John East
President and CEO, Actel Corporation

Download Your FREE Copy Of Libero® IDE
Integrated Design Environment

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Actel's New EV Devices Meet QML Class V Processing Specifications

Actel's new EV devices provide an even higher quality level for high-reliability systems used in space deployment.

By increasing its already stringent testing and screening process, Actel supports applications such as command and data handling systems, telemetry, attitude and station keeping, and spacecraft health systems. Actel's new EV production flow implements all of the steps specified by QML Class V. This is defined in the MIL-PRF-38535, a performance-based specification document that defines the general, quality assurance, and reliability requirements for the manufacture of integrated circuits intended for use in military and space applications.

RTAX-S Reliability White Paper
Download now

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Actel's Proven Low-Power Space-Flight Offerings

Actel is the leading provider of low-power FPGAs for high-reliability space applications. Over the last decade, Actel FPGAs have been onboard more than 100 launches and flown on over 300 satellites and spacecraft, including GPS-2RM, Mars Reconnaissance Orbiter, Mars Explorer Rovers 1 and 2 (Spirit and Opportunity), Echostar, and Globalstar.

RELIABILITY UPDATE

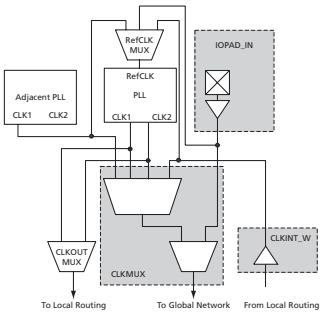
RTSX-SU Reliability Update

RTSX-SU FPGAs have now accumulated more than 5 million device hours in extended duration, extreme temperature reliability tests. An updated FIT calculator, developed by The Aerospace Corporation, is available from Actel Technical Support. The calculator predicts an antifuse FIT rate of approximately 25 for a typical RTSX-SU design. Further testament to the reliability of the RTSX-SU FPGA family comes from the successful deployment of RTSX-SU in multiple programs currently in flight, such as Mars Reconnaissance Orbiter, Pluto New Horizons, and multiple satellites in the GPS-2RM series.

RTAX-S Reliability Update

Extensive long-term testing on Axcelerator and RTAX-S FPGAs is still in progress. To date, more than 3 million device hours have been accumulated, and reliability of these low-power, antifuse-based devices has been exemplary. A FIT rate less than 7 FIT has been computed for these devices.

Download Answers to Your RTAX-S Clocking Questions



When should I use HCLKBUF vs. HCLKINT?

How do I assign global networks to I/O banks?

How do I implement global macros in HDL design?

How do I implement clock segmentation in RTAX-S devices?

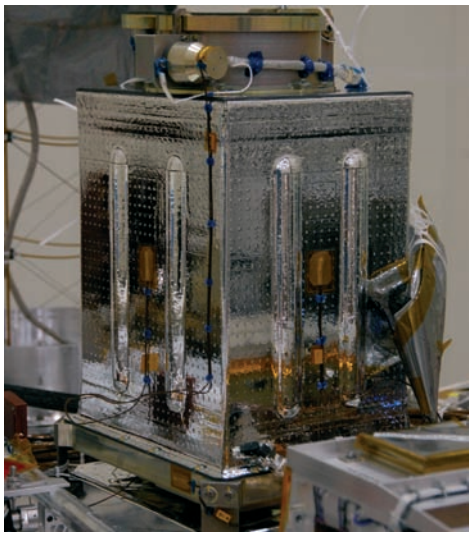
Download the SpaceWire Clock Recovery Application Note

actel.com/ezone/space07

RTAX-S Goes to Mars

First Low-Power FPGA Heads to Red Planet

The Phoenix spacecraft includes a Meteorological Station (MET), provided by the Canadian Space Agency.



MDA, a leading provider of robotic space systems, led construction of the MET instrument and has integrated Actel's one-million-gate RTAX1000S-CQ352 device into the instrument subsystem. The subsystem is used to acquire, process, and transmit temperature and pressure data to scientists and researchers back on Earth.

The Phoenix mission will study the history of water and habitability potential in the Martian Arctic's ice-rich soil. The Phoenix spacecraft includes the MET built by MDA, which will record the daily weather of the Martian northern plains using temperature and pressure sensors. Once the Phoenix arrives on Mars, the MET instruments will be used constantly in surface operations, which are expected to last 150 days. These instruments are central to scientific exploration on Mars, providing the essential tools scientists need to learn more about the Martian climate and geology and determine whether life has ever existed. The MET instrument will contribute to the success of the Phoenix mission.

The MET instruments operate on a combination of battery power and solar energy. Because sunlight in the Martian polar region is even weaker than at its equator, all systems and their components must feature extremely efficient power management.

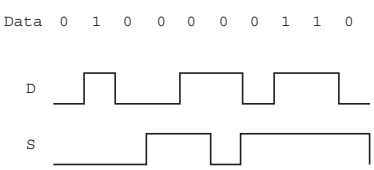
Actel's antifuse-based technology combines radiation tolerance with the industry's lowest power, enabling it to withstand the rigorous environments of space flight and exploration.

To learn more about the Phoenix Mission, visit http://phoenix.lpl.arizona.edu/.

SpaceWire Clock Recovery Logic Implementation

SpaceWire is a high-speed data link standard intended to meet the needs of future high-capability, remote sensing instruments in space missions.

SpaceWire provides a unified high-speed, data-handling infrastructure for connecting sensors, processing elements, mass-memory units, downlink telemetry subsystems, and Electrical Ground Support Equipment (EGSE). SpaceWire uses a Data-Strobe (DS) encoding scheme that encodes the transmission clock with the data into Data and Strobe so that the clock can be recovered by simply XORing the Data and Strobe lines together.



Data-Strobe Encoding

The Data signal (D) follows the data bitstream—high when the data bit is 1 and low when the data bit is 0. The Strobe signal (S) changes state whenever the Data does not change from one bit to the next.

One of the challenges when implementing SpaceWire in an FPGA is the implementation of the SpaceWire clock recovery circuit, which requires minimum timing of propagation delays. Using Actel's block methodology, the SpaceWire clock recovery circuit can be implemented and analyzed for minimum delay reliably in the RTAX-S device. The SpaceWire clock recovery circuit block can then be imported into the main design with identical timing delays.

When considering implementation of SpaceWire in an FPGA, the designer should make sure that the FPGA supports the LVDS I/O standard. Actel RTAX-S supports multiple I/O standards, including LVDS, which allows implementation of SpaceWire and other blocks with different I/O standards in the same FPGA.

Simulating SEU Events in Actel EDAC RAMs

Actel's designed-for-space RTAX-S low-power FPGAs provide embedded user static RAM in addition to single-event-upset (SEU)-enhanced logic.

The SEU-enhanced logic consists of triple-module-redundant (TMR) registers embedded in the silicon. However, the embedded user SRAM does not include any embedded mitigation capabilities. The integrity requirement of the data contained within the embedded SRAM is determined by the particular application and may range from non-critical, such as the pixel data for an image, to very critical, such as a header for a communication packet or a data word for a control application. Designers must determine whether the EDAC core is required in their application. If so, they must determine the configuration of the EDAC core, as well as how the remainder of the design should respond to the notification of an SEU event.

Implementing the SRAM blocks in conjunction with the Actel EDAC core can significantly improve the SEU performance of these embedded SRAM blocks for critical data applications. While the Actel EDAC core provides mitigation and/or notification of SEU-induced errors within the embedded SRAM memories, verifying the user control logic associated with an SEU-induced error is challenging because the user must induce an error that simulates a cosmic event.

Actel uses the functions of the Model*Sim*® AE simulator, included in the Actel Libero IDE tool suite, to quickly and easily accomplish this verification by mimicking one or more SEU events in the SRAM. One of the capabilities included in the Model*Sim* simulator is the ability to force a value onto a node within the design, until a new event triggers a new value to be driven onto that same node. The **Simulating SEU Events in EDAC RAM** application note describes how to use this Model*Sim* feature.

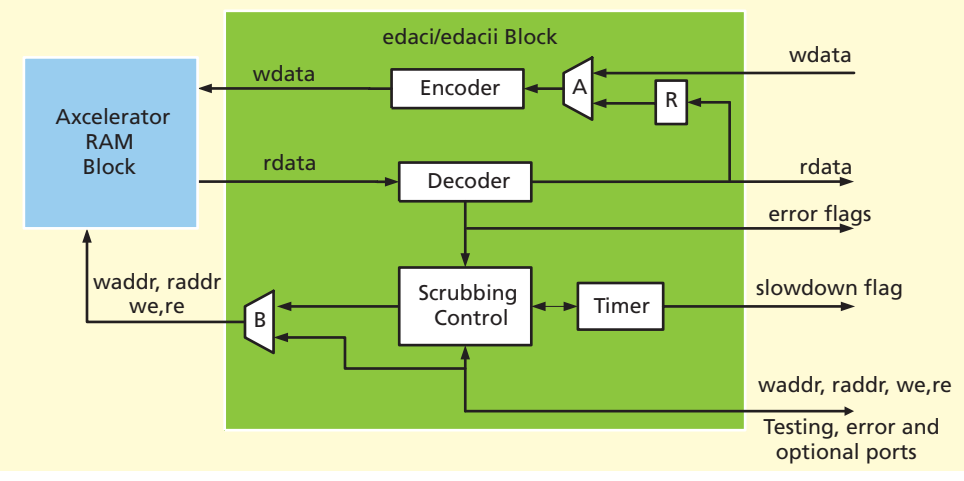
Test configuration options are dependent on the configuration of the EDAC core. In each case, certain levels of simulation are possible as described below:

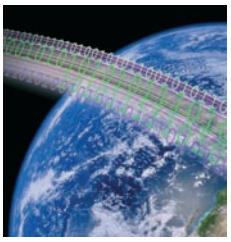
EDAC memories with no Error Flags or Test Ports
SEU events can be simulated, but observability is limited to verifying that the read data in the simulation is correct for one "induced SEU" event and is incorrect for two "induced SEU" events.

EDAC memories with Error Flags
SEU events can be simulated. In addition to observing the correct data for one "induced SEU event," the Corrected signal will indicate that the EDAC core found and corrected an error in the SRAM data. In the case of two "induced SEU events", not only will the read data be incorrect but the Error signal will also indicate that the EDAC core found an uncorrectable error.

EDAC memories with Error Flags and Test Ports
SEU events can be simulated and observed at the data word, Error signal, or Corrected signal. Additionally, the Test ports are available if the user wants to add simulation vectors to manipulate the parity bits of the coded word.

Functional Diagram of EDAC RAM

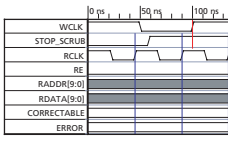




Using EDAC RAM for RadTolerant RTAX-S/SL

Application Note and Design Files

actel.com/ezone/space07



Simulating SEU Events in EDAC RAMs Application Note

actel.com/ezone/space07

Designing with RTAX-S Low-Power FPGAs

At this year's ASF, Jonathan Alexander, Senior Manager for Applications Engineering at Actel, presented solutions and recommendations for several of the most common questions and issues faced by designers using RTAX-S devices. Topics spanned all aspects of RTAX-S design, such as tool usage, programming, prototyping, device interface, and device characterization.

Download Top Design Tips for RTAX-S

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Actel has implemented a system that allows you to receive personalized notification on documentation changes. After you have registered, select products of interest from a list of silicon, IP, and tools. Every two weeks, Actel sends notifications that list new or updated document postings, based on products you selected. You can also filter this view for one month or three months, if you haven't visited in a while.

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Gaisler Fault-Tolerant LEON3 Processor for Actel's RTAX2000S FPGAs

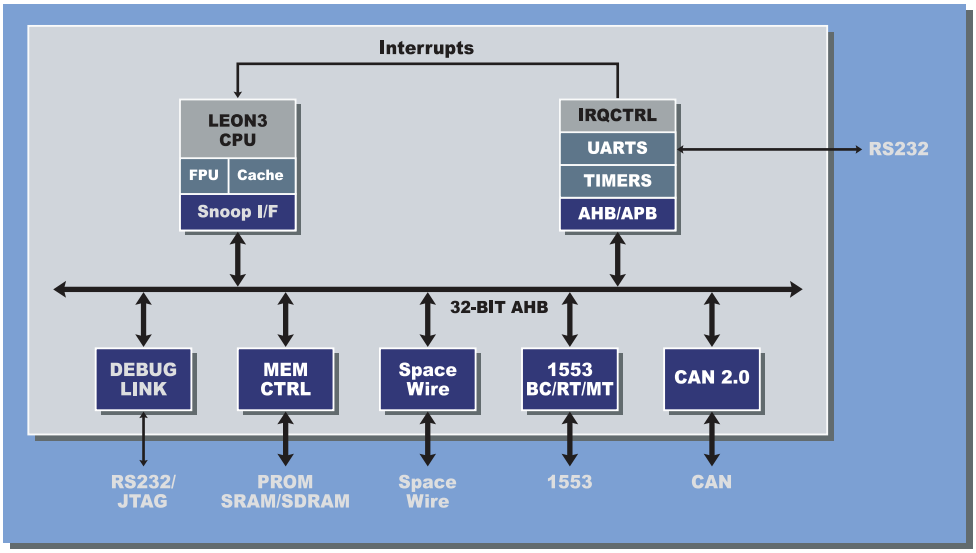
Combining the fault-tolerant LEON3 processor with Actel's radiation-tolerant RTAX2000S FPGA presents a competitive alternative to the processors currently used by the space industry.

At the Actel Space Forum, Gaisler presented details of the core, configurations, and performance, as well as discussed SEU mitigation techniques and the results of radiation tests performed by Gaisler Research. **View the ASF Proceedings.**

The LEON3-FT is available in four different configurations tailored for spacecraft and instrument control. Other configurations are available by request. The components are pre-programmed into the RTAX-S devices and shipped with a complete datasheet and user's manual.

LEON3FT-RTAX will be used on the Taiwanese **ARGO**, the Swedish **PRISMA** missions, and in the **BELA** instrument, which is a laser altimeter, chosen to be a payload on the European Space Agency **BepiColombo** spacecraft.

For LEON3, visit:
actel.com/ezone/space07

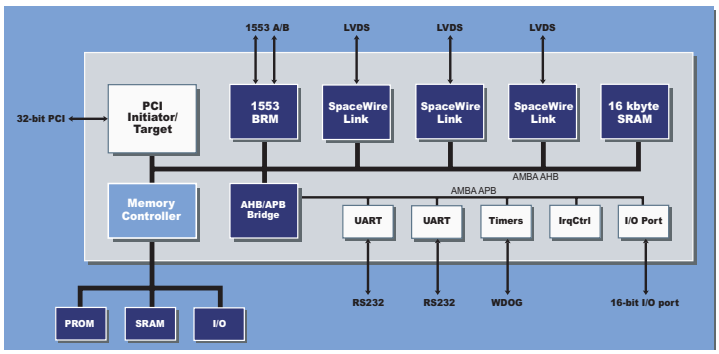


Gaisler PCI to SpaceWire and 1553 Bridge

In addition to the LEON3-FT implementation on RTAX-S, Gaisler also offers a companion chip for space processors and systems with a PCI interface implemented on RTAX2000S.

The GR701A PCI to SpaceWire and 1553 Bridge has been developed as a companion chip for the **AT697 SPARC V8 processor** and other systems with PCI interfaces. The chip provides a complete solution with three SpaceWire links, redundant MIL-STD-1553B interfaces, redundant CAN-2.0 interfaces, two UARTs, I/O ports, and interface to external memory. All the blocks and interfaces are currently used in European and US space programs and have been successfully validated and qualified. The MIL-STD-1553B and PCI blocks make use of Actel IP cores, whereas all other blocks, including the SpaceWire, are designed by Gaisler Research.

The GR701A is available as a standard component using the Actel RTAX2000S FPGA. The design is fault-tolerant and, in combination with the radiation-tolerant FPGA, this gives total immunity to radiation effects. This makes the GR701A ideally suited for space and other high-reliability applications.



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Equivalence Checking for FPGA Design

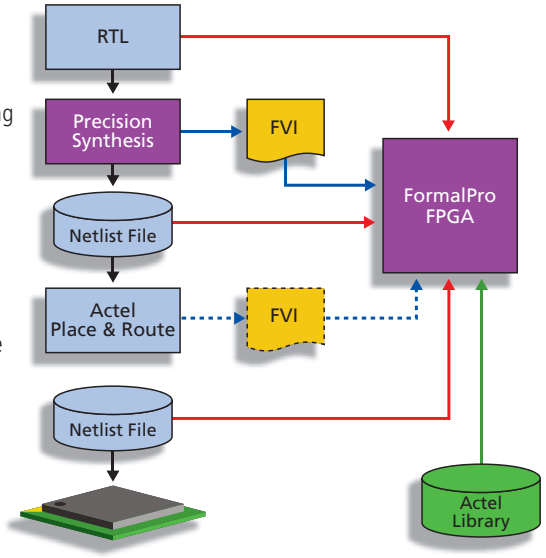
As FPGA designs have grown into the millions of gates, the task of verifying such large designs has become increasingly tedious.

Gate-level simulation with a typical design testbench is often not sufficiently exhaustive to provide good coverage, but the effort to create an exhaustive testbench is not only Herculean, but would also result in lengthy simulation times. By adopting ASIC verification techniques, FPGA designers can use equivalence checkers, such as FormalPro™, to quickly verify designs with 100% coverage, thereby keeping projects on schedule and error-free.

Synthesis and equivalence checking tools can work together to accelerate the verification process, enabling 100% gate-level verification of complex FPGA designs. Equivalence checking takes a gate-level implementation of a design and compares its functionality to that of a reference model of the same design.

The reference model is either the RTL model of the design or a known correct gate-level implementation. Formal verification tools, such as the Mentor Graphics® FormalPro equivalence checker, use formal proof algorithms to mathematically prove, or disprove, that the two versions are functionally identical.

View excerpts from Mentor Graphics white paper Equivalence Checking for FPGA Design.



Reprogrammable RTAX-S Prototyping

Allows Designers to Use Flash-Based FPGAs

The Aldec/Actel RTAX-S prototyping solution allows aerospace customers to take advantage of Actel's flash-based reprogrammable ProASIC3/E devices for flexible flash-based prototypes.

This new tool allows rapid reconfiguration of development platforms for space-flight computing, permitting faster integration and co-development of hardware and software. As part of the solution, a prototyping adaptor is provided, which maps the footprint of Actel's ProASIC3/E device to the footprint of a radiation-tolerant RTAX-S low-power device. As a result, customers can use the reprogrammable prototyping tool without altering the layout of their space-flight printed circuit board (PCB).

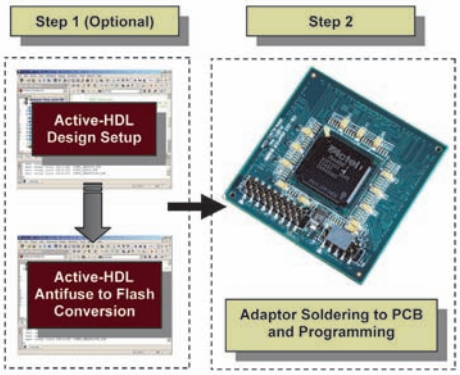
Available now, the complete prototyping solution includes an adapter board, programming kits, and the hardware and software tools needed for design conversion, mixed VHDL and Verilog simulation, mapping, and programming. Pricing is dependent on the target space-optimized RTAX-S device and package.

ALDEC
The Design Verification Company

Review Partner solutions with Aldec: http://www.aldec.com/solutions/actel/

The Aldec prototyping solution supports the following Actel devices:

- ProASIC3 device A3P1000-FG484 chip to CQ352 package
- ProASIC3E device A3PE1500-FG484 chip to CQ352 package
- All RTAX-S low-power devices are supported by the CQ352 package.



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eZone single-chip FPGA news

Featured in this issue:

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SpaceWire Clock Recovery Logic Implementation

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FPGA Equivalence Checking

LEON3-FT Processor

PCI to SpaceWire Bridge

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